



Low- Power: 25 μ A at low frequencies

A large portion of handheld applications have a 32 kHz standby mode in order to meet green power requirements. Most FPGA solutions today require some form of power-down mode, with an associated recovery time that ranges from us to ms. iCE devices allow applications to run in standby mode and monitor external stimuli such as keyboard clicks to wake up. There is no recovery time and the application responds instantaneously

Low- Cost: 65/40 nm Process

iCE devices use a silicon proven standard CMOS manufacturing process, allowing any foundry to manufacture the device. As no process customization is needed, manufacturing costs are reduced. 65/40 nm dies are significantly smaller than 130/90 nm dies. This results in more chips per wafer, hence, lower cost and power consumption.

ULTRA LOW-POWER iCE FPGAs

INTRODUCTION

Historically, the ultimate objective in the semiconductor industry has always been to make things bigger (in terms of functional capability), smaller (in terms of physical size), faster, more powerful, and cheaper. In the portable space and the handheld market segment, low power comes into play as the most critical feature. Explosive growth in the consumer market has drastically changed the requirements placed on silicon suppliers. Battery-life, enhanced feature sets, and changing standards are the new prime movers in electronic design. This market, although well served by FPGAs has been ignored by mainstream FPGA vendors. iCE is a new ultra low-power, low-cost, reprogrammable, non-volatile, SRAM based FPGA that provides an ideal platform for building consumer and handheld applications.

POWER CONSUMPTION IN FPGAs

Today, power concerns are at the forefront of FPGA design considerations and they are not limited to high-end devices. The new generation of low-cost FPGA families are all aimed at high-volume, low-cost applications. The target systems for these devices often run on batteries or have limited cooling capability or restricted power supplies, which makes lower power operation an absolute necessity. Specifically targeting handheld, battery-powered applications, Silicon Blue's iCE device holds the title as the lowest-power full-FPGA device. In planning the power budget for an FPGA design, there are three types of power consumption to consider: startup power, dynamic power, and static power.

STARTUP POWER

Startup power has two components that require consideration. As VDD ramps up to the correct voltage, the unknown state of SRAM cells on an SRAM-based FPGA can cause a current spike known as inrush current. This inrush current has been drastically improved over the past few generations of FPGAs by careful attention to power-up sequencing, but still it can rise to a level that warrants designer attention. The second startup hit in SRAM FPGAs is the increased current draw during the configuration process as the routing and look-up table (LUT) configurations are read from memory into the device.

After an SRAM FPGA has completed its initial power-up and reset, it must also be configured. During configuration, a bitstream is downloaded to the device and the various configuration bits are programmed. This process can take hundreds of milliamps and last for hundreds of milliseconds. The configuration current can prove to be lethal for battery-based applications where constant loads are desirable to maximize battery life. Typical SRAM based FPGAs exhibit high inrush and configuration current while iCE FPGA shows a maximum of 1.2mA of inrush current under a normal load. This proves to be highly effective for battery powered applications and makes iCE device the prime candidate amongst all SRAM based FPGAs for low-power portable applications.

DYNAMIC POWER

Dynamic power is the energy that is consumed by the device when it is doing actual work. Dynamic power is caused by transistors switching current in logic gates. Dynamic power then depends on the power consumption for logic cells. Power consumption includes internal resources like the number of logic cells/RAMS block used, operation clock frequency, toggle rates, routing and I/O power. For I/O power consumption, factors include output types, operating frequency, number of outputs toggling at once, and output load. The actual power consumption depends on the actual system design.

STATIC POWER

Static power is based on the current that is drawn by the FPGA when it is powered up, configured, and doing no work. Deep within the FPGA, transistors leak current even when they are not switching. This leakage increases when moving to smaller process geometries. As the number of transistors on a device goes up, the leakage increases. With Silicon Blue's patented technology, IC routing was optimized for a minimum leakage current. Portions of the circuitry are disabled when not used thus minimizing the effect of leakage on power consumption. Other FPGA vendors tend to sacrifice power for performance by not optimizing to minimize leakage.

Silicon Blue takes advantage of the 65nm Low Power process using its patented technology and by using low-leakage type transistors.

POWER VS. FREQUENCY

Silicon Blue low power FPGAs can operate from 1.0V core and consume 50% less static power and over 50% less dynamic power than 1.8 V “low-power” PLD alternatives. In running benchmarks by filling each of our competitors FPGA with 192 16-bit counters (3.5K worth of LUTs) and then comparing their performance against the iCE device, we found that the iCE device offers the lowest-power versus frequency, even when compared to flash and antifuse based devices from the same class. Below is a graph that represents the power versus frequency curve in all major FPGA devices.

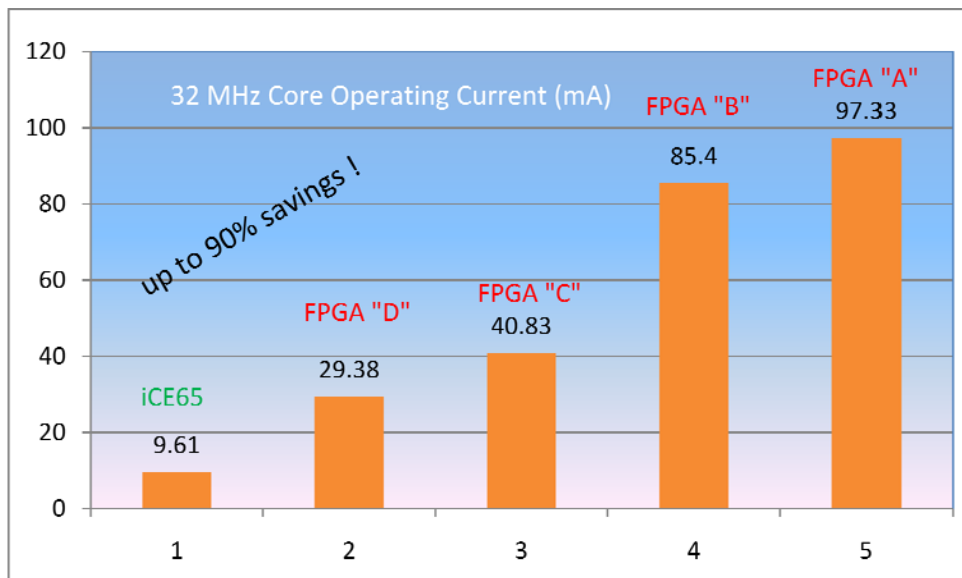
Figure 1: Power versus Frequency for 192 16-bit counter design

The table below shows the core voltage, power consumption and operating current at 32 kHz and 32 MHz. The iCE65 offers outstanding performance compared to other FPGAs in the same class. The low operating voltage and the patentable technology used in circuit design puts the iCE device at the forefront of true low-power FPGAs on the market.

Table 1: Core Power and Operating Current at 32 kHz and 32 MHz

	iCE65LP	FPGA "A"	FPGA "B"	FPGA "C"	FPGA "D"
Core Voltage	1.2V	1.8V	1.8V	1.5V	1.2V
Power at 32 kHz (mW)	0.061	0.33	0.50	35.03	0.18
Power at 32 MHz (mW)	11.53	175.20	153.72	61.24	35.25
I _{dd} at 32 kHz (mA)	0.051	0.18	0.28	23.35	0.15
I _{dd} at 32 MHz (mA)	9.61	97.33	85.4	40.83	29.38

iCE65 offers true ultra low operating current compared to other FPGAs. At 32 MHz, operating current can be lower by as much as 90% than a competitor's FPGA.



The graph below shows the iCE4 core operating I_{dd} versus frequency. Even at frequencies close to 100 MHz, the relative core operating current is within 10mA. Total power consumption in the case of using 192 counters of 16-bits is close to 18mW beating every other FPGA device available today on the market

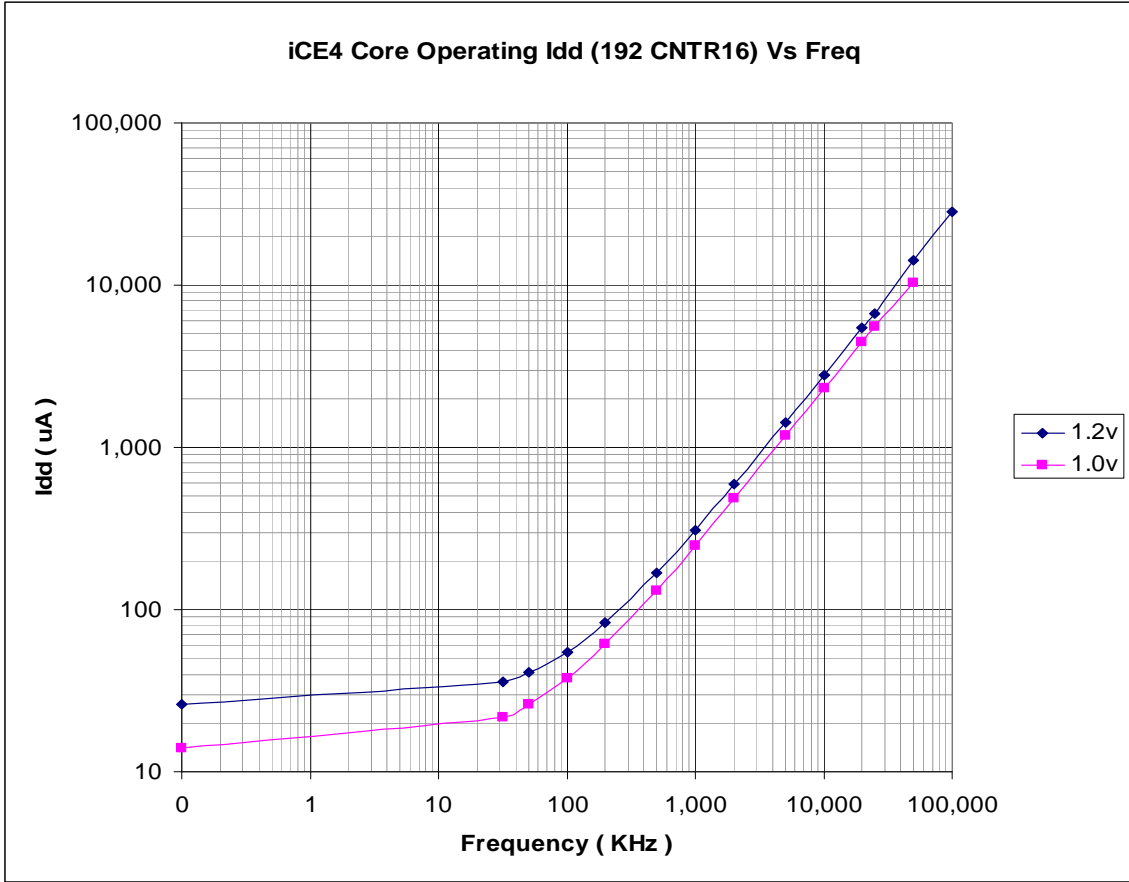


Figure 2: iCE4 Core Operating Idd

POWER ESTIMATION

On the software tool side, Silicon Blue offers software to help handheld applications designers estimate power consumption. Using a simple spreadsheet system, designers can estimate their device’s power consumption based on their design considerations. Users supply estimates of design parameters such as logic, memory, and I/O utilization, and clock frequencies, and the tool provides an estimate of power consumption for these conditions. While these estimates may not be completely accurate they are very useful for designers to use them as basis in deciding which implementation works best for their FPGA design. You can download the power estimator spreadsheet from www.siliconbluetech.com

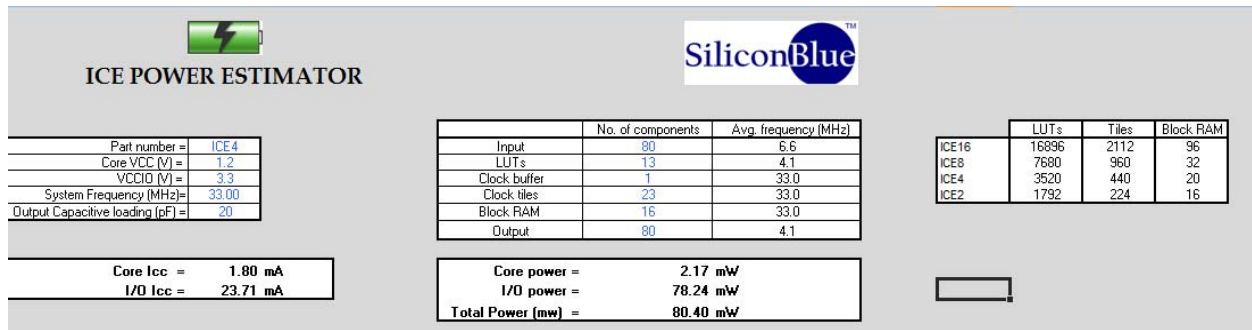


Figure 3: ICE Power Estimator

SUMMARY

Silicon Blue offers the lowest-power SRAM based FPGA devices on the market. With its integrated configuration memory technology, Silicon Blue answers a long-time absence for an ultra-low power, non-volatile SRAM based FPGA that is targeted toward battery-powered systems.