Dual-Row QFN Package Assembly and PCB Layout Guidelines

SiliconBlue®

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Introduction

Leadless Quad Flat Pack (QFN) packages are plastic-encapsulated with a copper lead frame substrate, providing a robust, low-cost solution for small form factor applications such as mobile handsets and other battery operated consumer products. Dual-row QFN packages have interstitial, staggered contacts. The inner row is offset 0.5 mm, resulting in a compact design that does not exceed the surface mount technology (SMT) capability of a typical 0.5 mm pitch surface-mount process.

Because SiliconBlue iCE65 mobileFPGA devices have the ultra-low power consumption, connecting the center thermal pad is not required. Therefore, when designing a PCB for an iCE65 mobileFPGA in the QN84 package, the following primary factors can affect the successful package mounting on the board:

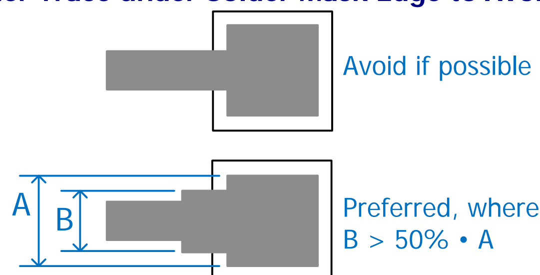
- **Perimeter Land Pad and Trace Design**
- **Stencil design**
- **Type of vias**
- **Board thickness**
- **Lead finish on the package**
- **Surface finish on the board**
- **Type of solder pasted**
- **Reflow profile**

These are general guidelines and other factors may affect the successful and reliable mounting of a QN84 package. Additionally, particular applications may require specific analysis and/or considerations that are not covered here. All spacing calculations assume a standard four-layer board using one-half ounce of copper.

Perimeter Land Pad and Trace Design

In several published QFN tests, trace cracking was observed during board-level drop and bend tests. The reported trace cracking usually occurred at the edge of the solder mask opening around the metal pad. To avoid this failure mode, widen the trace under the solder mask edge so that it is wider than the remainder of the trace as shown in Figure 1. Depending on the reliability requirements, the wider part of the trace might need to be as wide as 50 to 75% of the metal pad width.

Figure 1: Wider Trace under Solder Mask Edge to Avoid Trace Cracking



Non-solder mask defined (NSMD) pads are recommended for dual-row QFN packages, because the copper etching process has tighter control than the solder masking process and improves the reliability of the solder joints.

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Stencil Design for Perimeter Land Pads

For reliable solder joints on dual-row QFN packages, pay extra attention because of the small land surface area and the sole reliance on printed solder paste on the PCB surface. Special considerations are needed in stencil design and paste printing for both perimeter lands. Because the surface mount process varies from company to company, careful process development is recommended. The following section provides some guidelines for stencil design based on industry experience.

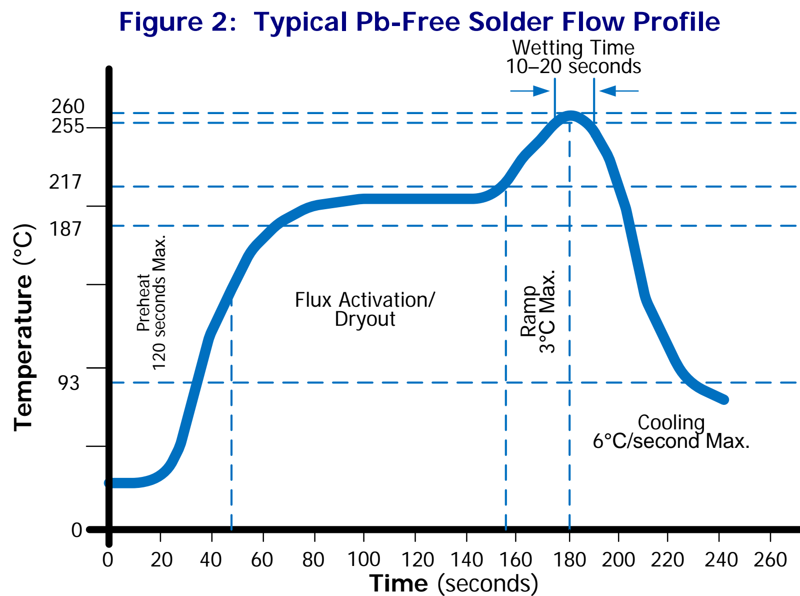
The optimum and reliable solder joints on the perimeter pads have about 50 to 70 µm (2 to 3 mils) standoff height. Tightly control the stencil aperture tolerance because these tolerances can effectively reduce the aperture size. Area ratios of 0.66 and aspect ratios of 1.5 were never exceeded. The land pattern on the PCB should be 1:1 to the land pads on QFN package.

Stencil thickness of 0.125 mm is recommended for 0.5 mm dual-row QFN packages. A laser-cut stainless steel stencil with electro-polished trapezoidal walls is recommended to improve the paste release. SiliconBlue recommends that no-clean, Type 3 or Type 4 paste be used for mounting QFN packages. Nitrogen purge is also recommended during reflow.

Reflow Profile

Reflow profile and peak temperature have a strong influence on void formation. SiliconBlue strongly recommends that users follow the profile recommendation of the paste suppliers, since this is specific to the requirements of the flux formation. However, the following profile, Figure 2 serves as a general reference for SiliconBlue mobileFPGA devices.

Figure 2: Typical Pb-Free Solder Flow Profile



Assembly Process Flow

QFN packages use the same process flow used for typical surface mount packages, without modification. Include post-print and post-reflow inspections, especially during initial process refinement. The paste volume should be approximately 80%–90% of stencil aperture volume to indicate sufficient paste release and should be measured either by 2D or 3D techniques. After reflow, inspect the mounted packages for the presence of voids, solder balling, or other defects. Cross-section analysis may be required to determine the fillet shape and size and joint standoff height.

Rework Guidelines

Since solder joints are not fully exposed, retouch work for QFN packages is limited. For defects underneath the package, the entire device must be removed. In addition, rework of QFN packages after removal can be a challenge due to their small size. Also, since QFN devices are typically mounted on smaller, thinner, and denser PCBs, handling and heating can be problematic. Because of these complexities, the following guidelines provide a starting point for the development of a successful rework process for these packages.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste application
4. Component placement and attachment

The first step to remove the component is the reflow of solder joints attaching the component to the PCB board. Ideally the reflow profile for removing the component should be the same as the one used for part attachment. However, the time above liquid can be reduced as long as the reflow is completed. In the removal process, the board should be heated from the bottom side using a convective heater, and hot gas or air should be used on the top side of the component. A special nozzle should be used to direct the heating in the component area. The heating of adjacent components should be minimized. Air velocity of 15 to 20 liters per minute is a good starting point, and excessive airflow should be avoided. Once the joints have reflowed, the vacuum lift-off should be automatically engaged during the transition from reflow to cool down. Because of their small size, the vacuum pressure should be kept below 15 inches of mercury (Hg). This will ensure the component is not lifted if all joints have not been reflowed, thus avoiding pad liftoff.

After the components have been removed, the site must be cleaned properly. Use a combination of a blade-style conductive tool and de-soldering braid. Match the width of the blade to the maximum width of the footprint and set the baked temperature low enough so as not to cause any damage to the circuit board. Once the residual solder is removed, clean the landing pads with solvent. The solvent is usually specific to the type of paste used in the original assembly and follow the paste manufacturer's recommendations.

Because of their small size and finer pitches, solder paste deposition for QFN packages require extra care. Use a miniature stencil specific for the component to achieve a uniform and precise deposition. Align the stencil aperture with the pads under 50X–100X magnification. Then, lower the stencil onto the PCB and deposit the paste with a small metal squeegee blade. Alternatively, use miniature stencil to print paste on the package site. Use a stencil with a thickness of 125 µm with an aperture size and shape the same as the package land. Use no-clean flux because the small standoff of QFN packages does not leave much room for cleaning.

QFN packages have superior self-centering ability due to their small mass. Placing QFN packages is similar to BGA package placement. Because the land pads are on the underside of the package, use a split-beam optical system to align the component onto the motherboard. This optical system forms an image of land overlaid on the mating footprint and aid proper alignment. Again, perform the alignment at 50X–100X magnification. The placement machine should be capable of allowing fine adjustments in X, Y, and rotational axes. Use the reflow profile developed during the original component attachment or removal process to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile eliminates the need for thermocouple feedback and reduces operator dependencies.

Other Documentation

See also the single-layer layout example for the QN84 package in the following application note.

- **AN010: iCE65 Printed Circuit Board (PCB) Layout Guidelines**
  www.siliconbluetech.com/media/downloads/SiliconBlue_AN010.pdf

Appendix I: Recommended PCB Layout Details

Figure 3 shows the suggested board layout for the QN84 package on a top layer of a printed circuit board, assuming NSMD solder mask rules. The labeled dimensions are listed in Table 1.

Figure 3: Top-layer Layout

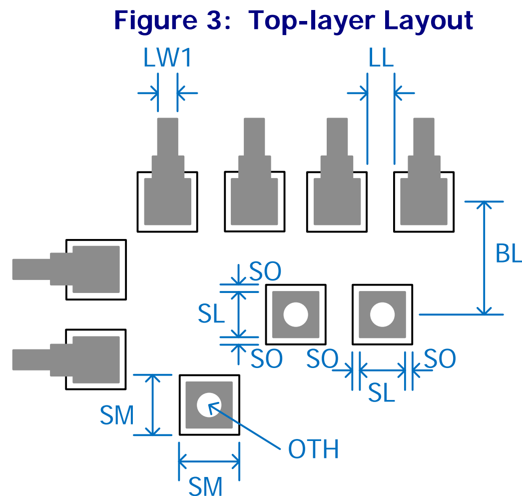


Figure 4 shows the suggested layout if pads are connected on inner layers.

Figure 4: Inner-layer Layout

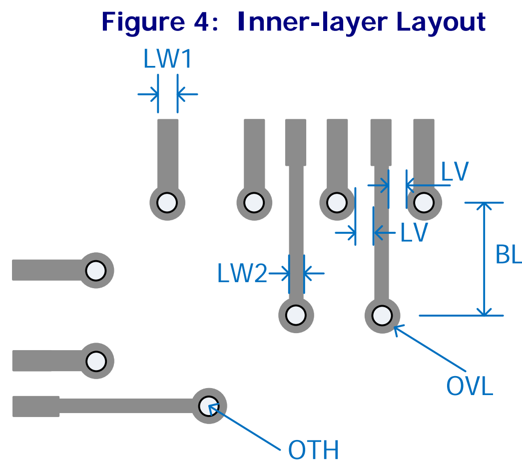


Table 1: Recommended dimensions for QN84 package

Dimension	Symbol	QN84	Units
Component Land Pad Diameter	SMD	0.300	mm
Solder Land Diameter	SL	0.300	
Solder Mask Opening Diameter	SM	0.425	
Solder Land to Solder Land	LL	0.075	
Solder Mask Overlap	SO	0.0625	
Package Pin Pitch		0.500	
Solder Land Pitch	BL	0.650	
Line Width between Via Outside and Via Land	LW1	0.127	
Line Width between Via and Via Land	LW2	0.100	
Line to Via Land	LV	0.050 – 0.100	
Via Land Diameter	OVL	0.250 – 0.400	
Via Opening Diameter	OTH	0.100 – 0.250	

Revision History

Version	Date	Description
1.0	9-AUG-2010	Initial release.

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