

iCE40 “Los Angeles” mobileFPGA Family

Advanced Information		LP Series (Low Power)					HX Series (High Performance)				
Features		LP640	LP1K	LP4K	LP8K	LP16K	HX640	HX1K	HX4K	HX8K	HX16K
Logic Cells		640	1,280	3,520	7,680	16,192	640	1,280	3,520	7,680	16,192
Embedded RAM Bits		32K	64K	80K	128K	384K	32K	64K	80K	128K	384K
Phase-Locked Loops		1	1	2	2	2	1	1	2	2	2
Core Power @ 0 KHz ¹		15 μ W	20 μ W	70 μ W	80 μ W	150 μ W	120 μ W	160 μ W	400 μ W	660 μ W	1500 μ W
Package ²	Footprint	User I/O (Differential Pairs)									
CM36 ³	2.5x2.5mm	25 (3)	25 (3)								
CM49	3x3 mm	35 (5)	35 (5)								
CM81	4x4 mm	63 (8)	63 (8)	63 (9) ⁴							
CM121	5x5 mm		95 (12)	93 (13)	93 (13)						
CM225	7x7 mm			167 (20)	178 (23)	178 (23)				178 (23)	
QN84 ³	7x7 mm		67 (7)								
CB132	8x8 mm							97 (11)	95 (12)	95 (12)	
CB284	12x12 mm										222 (25)
CT256	14x14 mm									206 (26)	206 (26)
VQ100 ³	14x14 mm						67 (8)	72 (9)			
TQ144	20x20 mm							96 (12)	107 (14)		

Note 1: At 1.0V VCC

Note 2: Packages: CB–0.5 mm pitch Chip-Scale Ball Grid Array, CM–0.4 mm pitch Chip-Scale Ball Grid Array, CT–0.8 mm pitch Ball Grid Array, TQ–Thin Quad Flat Pack, VQ–Very Thin Quad Flat Pack

Note 3: No PLL Available

Note 4: Only 1 PLL Available

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