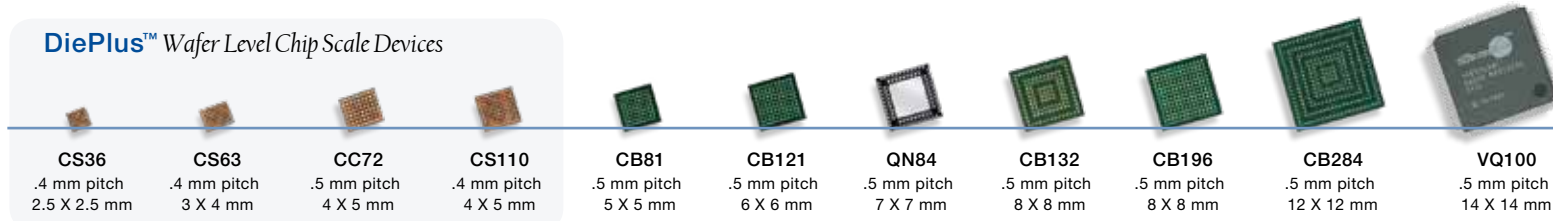


# The iCE65 mobileFPGA family

	<b>L-Series</b> Optimized for ultra-low power applications (1.0 Volt and 1.2 Volt Operation)								<b>P-Series</b> Optimized for display, memory and SERDES applications (1.2 Volt Operation)		
<b>PART NUMBER</b>	<b>L01</b>		<b>L04</b>		<b>L08</b>		<b>L16<sup>1</sup></b>		<b>P04</b>	<b>P08<sup>1</sup></b>	<b>P16<sup>1</sup></b>
Logic Cells	1,280		3,520		7,680		16,896		3,520	7,680	16,896
System Gate Equivalent	60K		200K		400K		800K		200K	400K	800K
Embedded RAM Bits	64K		80K		128K		384K		80K	128K	384K
Embedded RAM 4K Blocks	16		20		32		96		20	32	96
Phase-Locked Loop	0		0		0		0		1	2	2
Power/Speed Grade (-L@1.0V, -T@1.2V)	-L	-T	-L	-T	-L	-T	-L	-T	-T	-T	-T
Core Operating Current, 0 KHz	12 $\mu$ A	19 $\mu$ A	26 $\mu$ A	43 $\mu$ A	54 $\mu$ A	90 $\mu$ A	TBD	TBD	43 $\mu$ A	TBD	TBD
Core Operating Current, 32 KHz	15 $\mu$ A	23 $\mu$ A	31 $\mu$ A	50 $\mu$ A	62 $\mu$ A	100 $\mu$ A	TBD	TBD	60 $\mu$ A	TBD	TBD
Core Operating Current, 32 MHz	3 mA	4 mA	7 mA	8 mA	14 mA	17 mA	TBD	TBD	9 mA	TBD	TBD
Configuration Bits	245K		533K		1,057K		TBD		533K	TBD	TBD
<b>PACKAGE</b>	<b>PROGRAMMABLE I/O: MAX I/O (LVDS CHANNELS)</b>										
81-ball BGA	63 (0)										
84-pin QFN	67 (0)										
100-pin VQFP	72 (0)		72 (9)								
121-pin BGA									95 (13)		
132-ball BGA	93 (0)		95 (11)		95 (12)						
196-ball BGA			150 (18)		150 (18)				148 (18)		
284-ball BGA			176 (20)		222 (25)				174 (20)		
<b>DiePlus™ (Known Good Die)</b>	<b>PROGRAMMABLE I/O: MAX I/O (LVDS CHANNELS)</b>										
Wafer Level Chip Scale Package: WLCSP	CS36 25 (0)		CS63 48 (4)		CC72 55 (8)	CS110 92 (12)					
Bare Die	95 (0)		176 (20)		222 (25)				174 (20)		

Note 1: Consult Factory

## DiePlus™ Wafer Level Chip Scale Devices



Packages are shown actual size.