

iCE65 as CF+ Interface

Overview

CompactFlash(CF) is a mass storage device format used in portable electronic devices like digital cameras, PDAs and cellular phones etc.. For storage, CompactFlash typically uses flash memory in a standardized enclosure. The CF cards support only common memory data storage whereas the CF+ cards expand to include I/O devices such as Ethernet cards and also consumes less power. This design example illustrates the implementation of a CF+ interface using iCE65 FPGAs. As a CF+ interface, the iCE65 FPGA generates all the required interfacing signals and implements the functions that are required for such a system.

Description

The CF+ cards can be configured in three modes.

- Mode 1 is used to support PC Card ATA using I/O.
 - Mode 2 is for PC Card ATA using Memory.
 - Mode 3 is reserved for True IDE mode to ensure full compatibility with Disk Drives.
- This design example supports I/O mode and memory mode.

PC CARD ATA using I/O mode

This mode is used to interface with I/O cards like serial cards, Ethernet cards and wireless cards that uses the CF+ interface to operate. Using this part of the interface allows the host to exchange data with the I/O cards. The operations that can be carried out in this mode is :

- Byte Input/Output access
- Word Input/Output access
- Read/Write Inhibit
- High Byte Input/Output only

The I/O transfer to or from the CF+ Card can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CF+ Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CF+ Card, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds. CF+ cards may or may not allow 16 bit register accesses and thus shall assert -IOIS16 as required. The CF+ Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

PC Card ATA using memory mode

This mode is used to access the flash memory of the CF+ cards. The Common Memory transfer to or from the CF+ Card can be either 8 or 16 bits as desired by the host. This also includes the various configuration registers like the configuration option register, card status register, I/O base registers which can be addressed using this interface. The CF+ Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle. The operations that can be carried out in this mode is :

- Configuration option register read
- Configuration option register write
- Card status read
- Card status write
- Pin replacement register read
- Pin replacement register write
- Memory read/write (8 to 16 bits)

Implementation

The CF+ Interface implementation is based on CompactFlash specification version 4.0. Figure 1 shows the overall interface of CF+ controller to both host processor and CF+ device. A brief description of the interfacing signals are listed in Table 1.

The CF+ interface block monitors host side transaction requests to the CF+ card or the I/O card. Depending on the host processor request, the appropriate control signals are sent to the CF+ along with the address. The sequence of operation is as follows:

- Host processor pulls cs_n low and enables the CF+ card interface
- The pins cf_detect[1:0] goes low when CompactFlash card inserted into the socket
- CF+ Interface generates a low on cf_intr and communicates to the host processor that CF+ Interface is now activated
- Host generates a high on fn_write indicating to the Interface that the host is ready for data transaction
- All the transactions of the interface, CF+ card and host processor are synchronized with the fn_write signal.

On the rising edge of the fn_write, the FSM samples cf_fn_cntrl[4:0] pins. Each operation in both the modes is encoded with 5 bits specified by the controller using the cf_fn_cntrl pins. The FSM on every rising edge of fn_write decodes the cf_fn_cntrl line and generates the necessary control signals to carry out the requested operation successfully. The control signal being generated by the interface during memory operations is cf_we and cf_oe, while during I/O operations the control signals generated are cf_iord and cf_iowr. The other control signals generated by CF+ Interface are CF enable cf_ce1, cf_ce2 and memory enable cf_reg, which are common for both the modes of operation. The logic levels of these generated signals are defined as per the CF+ standard.

The host data bus [15:0] and card data bus[15:0] are connected to each other.

The fn_reset signal is generated by the host. On receiving this the interface generates the reset signal to the CF+ card and goes to the reset mode. The fn_reset generates a high on cf_reset(hardware reset) as well control signals necessary to configure the configuration registers for CF+ reset functionality

Table 1 describes the various ports on the CF+ Interface. Table 2 summarizes the post P&R resource utilization summary of this Design Example when implemented using iCE65 FPGA.

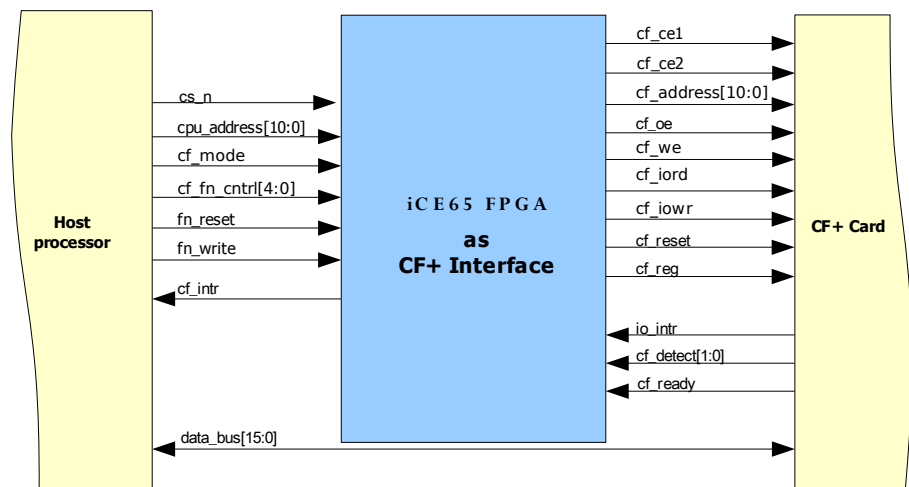


Fig 1: CF+ Interface

Pin	Direction	Description
cpu_address[10:0]	Input	Address bus from host
cf_mode	Input	Selection between I/O and memory mode operations
cf_fn_cntrl[4:0]	Input	Selection between I/O and memory read/write operations
fn_reset	Input	Active low Reset pin asserted by host
fn_write	Input	Rising edge generates control signals based on cf_fn_cntrl
cf_intr	output	Interrupt line to the host, Active low for card detect.
cf_ready	Input	Asserted low during power up or reset, and made high in the memory mode
cf_detect[1:0]	Input	Active low Card detect signals
io_intr	Input	Interrupt request from I/O Device
cs_n	input	Chip select
cf_reg	output	Low during I/O operations, used in memory mode
cf_reset	Output	Compact flash reset pin, Active High.
cf_iowr	Output	Active low I/O write select line
cf_iord	Output	Active low I/O read select line
cf_we	Output	Active low write enable line used to write to configuration registers
cf_oe	Output	Active low output enable line
cf_address[10:0]	Output	Address bus
cf_ce1	Output	Active low card select signal
cf_ce2	Output	Active low card select signal

Table 1: Pin Description

Device	Logic Cells	IO Cells
iCE65L04-UCB284	63	44

Table 2: Resource Utilization

Conclusion

This design example demonstrates the implementation of a CF+ interface using iCE FPGAs. iCE FPGA's very low power capabilities makes iCE FPGAs an obvious choice for implementing a CF+ interface for battery operated compact/handheld devices PDAs, cellular phones etc..

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