

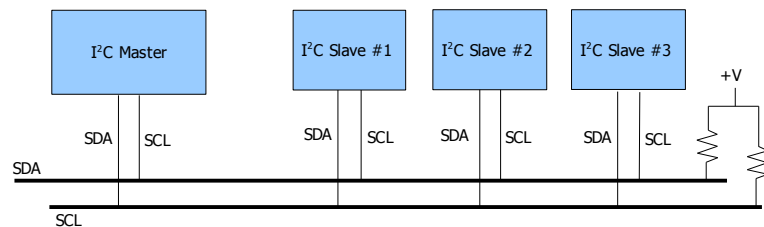
## iCE65 as I<sup>2</sup>C Master

### Overview

This design example illustrates the implementation of an I<sup>2</sup>C Master using SiliconBlue iCE65 FPGAs. The I<sup>2</sup>C Master implemented is capable of reading illumination data from an I<sup>2</sup>C Slave Illumination Sensor product such as Intersil's ISL29002.

### Description

I<sup>2</sup>C, or Inter-Integrated Circuit is a popular serial interface protocol that is widely used in many electronic systems. The I<sup>2</sup>C interface is a 2 wire interface capable of half duplex serial communication at moderate to high speeds of up to a few mega bits per second. The I<sup>2</sup>C system incorporates an addressing system to identify the multiple I<sup>2</sup>C 'Slaves' on the I<sup>2</sup>C bus. An I<sup>2</sup>C system can have single or multiple Masters. The two bidirectional lines of the I<sup>2</sup>C system are SDA (Serial Data) and SCL (Serial Clock). An important electrical feature of the I<sup>2</sup>C lines are that they are both made up of open-drain type of ports and are pulled high by resistors.



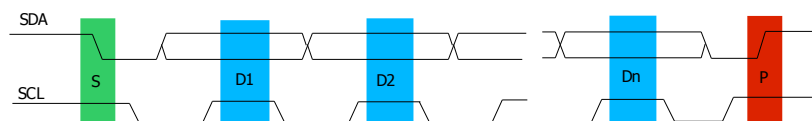
**Fig 1: A typical I<sup>2</sup>C system**

Fig 1 above shows a typical I<sup>2</sup>C bus system comprising of 3 Slaves and a single Master. An I<sup>2</sup>C data transaction always begins with a Start condition and ends with a Stop condition. Addresses to the Slave are typically 7 bit long, and a following 8th bit denotes a Read (when this bit = 1) or a Write (when this bit = 0) operation. An acknowledge bit is issued by the receiving party to acknowledge an 'in-order' transaction. The Slave also acknowledges when it's address has been received by it.

The following summarizes the main signal features of an I<sup>2</sup>C system:

- START (S): Falling edge of SDA when SCL is high
- STOP (P): Rising edge SDA when SCL is high
- WRITE: 7 bit Slave address appended by a '0' on the 8th bit
- READ: 7 bit Slave address appended by a '1' on the 8th bit

Fig 2 below shows a typical I<sup>2</sup>C timing diagram where a n bit serial data (D0 ~ Dn) is presented on the SDA line .

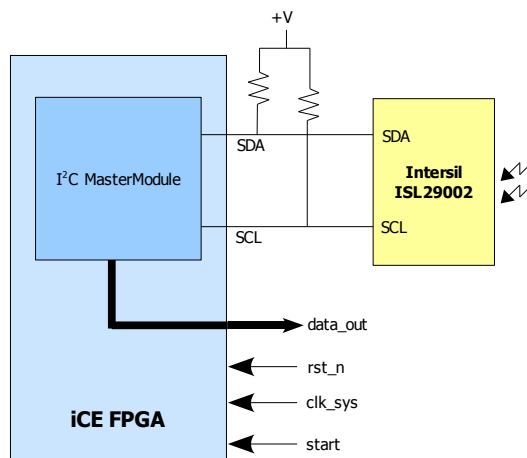


**Fig 2: A typical I<sup>2</sup>C timing diagram**

## Implementation

This design example configures the iCE as a I<sup>2</sup>C Master suitable to transact with a typical I<sup>2</sup>C Slave. As an example I<sup>2</sup>C Slave, an illumination sensor device by Intersil, the ISL29002 is considered. The iCE65 I<sup>2</sup>C Master thus configures the ISL29002 device per its requirements and reads illumination data sensed by it.

Fig 3 below illustrates the I<sup>2</sup>C Master Slave arrangement. The I<sup>2</sup>C Master is implemented in the iCE FPGA to suit the ISL29002 Slave device (data sheets of this device can be obtained from Intersil at <http://www.intersil.com/data/fn/fn7465.pdf>) The data obtained from the sensor Slave is presented at the 8 bit wide data\_out port. The Master provides the necessary Start condition, Slave addressing functions, Slave initialization functions and transacts data to and from the Slave.



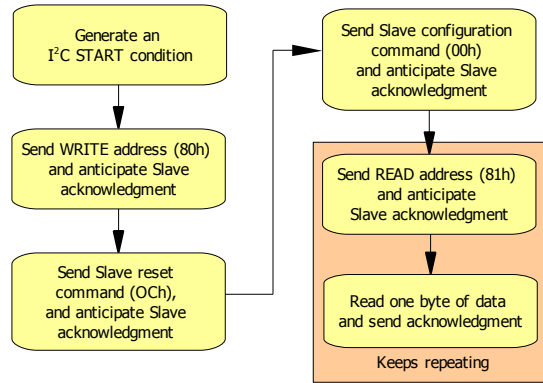
**Fig 3: I<sup>2</sup>C Master – Slave arrangement**

Port	Direction	Description
SDA	Inout	Open Drain type I <sup>2</sup> C serial data line
SCL	Inout	Open Drain type I <sup>2</sup> C serial clock line
data_out[7:0]	Output	8 bit wide data corresponding to the MSB of the 16 bit illumination sensor output
rst_n	Input	System Reset(active low)
start	Input	System enable, when '1' initiates data transaction, otherwise disables it
clk_sys	Input	System clock input, 12.28 MHz

**Table 1: Pin Description**

As can be seen in Fig 3, the implementation in the iCE FPGA includes the I<sup>2</sup>C Master and some more logic that initializes the Slave, issues commands to enable the sensor Slave to read illumination data and provides an output corresponding to the light sensed by the sensor. This is effectively combining the function of a Host system in addition to a specific implementation of an I<sup>2</sup>C Master.

Fig 4 in the following page indicates the sequence of events that are required in transacting illumination data from the I<sup>2</sup>C sensor Slave. This implementation has the 7 bit Slave address set to be 40h (1000 000). Appropriate delays, as required by the Slave are provided between commands and between successive READ operations. For details of the commands and other specific requirements of the ISL29002 device refer the device data sheets as mentioned above.



**Fig 4: I<sup>2</sup>C sequence flow involved in reading sensor**

Table 2 shows the post P&R resource utilization summary of this design when implemented using iCE FPGA.

Device	Logic Cells	IO Cells
iCE65L04-UCB284	217	15

**Table 2: Resource Utilization**

## Conclusion

This design example demonstrates the implementation of an I<sup>2</sup>C Master along with host functions on iCE FPGAs. I<sup>2</sup>C's intrinsic pin count and board real estate saving characteristics are well complemented by iCE FPGA's very low power capabilities. This makes iCE FPGAs an obvious choice for I<sup>2</sup>C Master applications in all low power, battery operated and compact applications.

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