May 2008
DE REF #304

iCE65 as I²C Slave: Port Expander

Overview

This design example illustrates the implementation of an I²C Slave using SiliconBlue iCE65 FPGAs. The I²C Slave implemented functions as a port expander via an I²C bus.

Description

I²C, or Inter-Integrated Circuit is a popular serial interface protocol that is widely used in many electronic systems. The I²C interface is a 2 wire interface capable of half duplex serial communication at moderate to high speeds of up to a few mega bits per second. The I²C system incorporates an addressing system to identify the multiple I²C 'Slaves' on the I²C bus. An I²C system can have single or multiple Masters. The two bidirectional lines of the I²C system are SDA (Serial Data) and SCL (Serial Clock). An important electrical feature of the I²C lines are that they are both made up of open-drain type of ports and are pulled high by resistors.

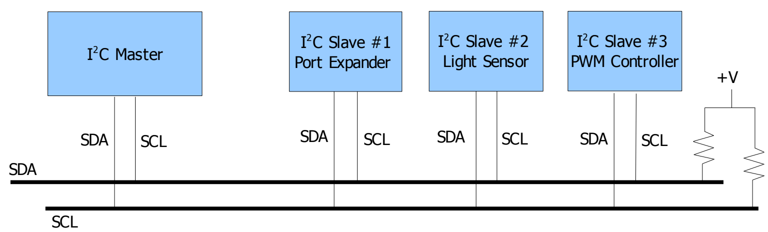

Fig 1: A typical I²C sysytem

Fig 1 above shows a typical I²C bus system comprising of 3 Slaves and a single Master. An I²C data transaction always begins with a Start condition and ends with a Stop condition. Addresses to the Slave are typically 7 bit long, and a following 8th bit denotes a Read (when this bit = 1) or a Write (when this bit = 0) operation. An acknowledge bit is issued by the receiving party to acknowledge an 'in-order' transaction. The Slave also acknowledges when it's address has been received by it.

The following summarizes the main signal features of an I²C system:
START (S): Falling edge of SDA when SCL is high
STOP (P): Rising edge SDA when SCL is high
WRITE: 7 bit Slave address appended by a '0' on the 8th bit
READ: 7 bit Slave address appended by a '1' on the 8th bit

Fig 2 below shows a typical I²C timing diagram where a n bit serial data (D0 ~ Dn) is presented on the SDA line .

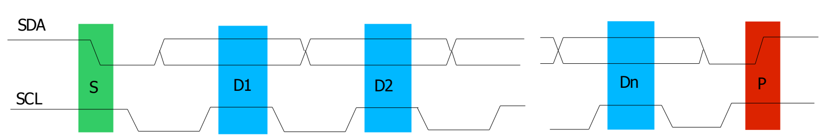

Fig 2: A typical I²C timing diagram

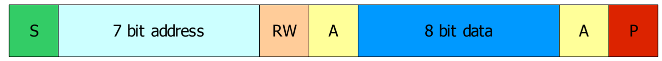

Fig 3: A typical I^{2}C signal format

Fig 3 above illustrates a typical I^{2}C signal format. The following denotes the components of such a format:

S: I^{2}C START condition
7 bit address: The 7 bit Slave address
RW: READ / WRITE signifying bit; ('0' for Write, '1' for Read)
A: Acknowledge bit; is set to low to indicate an acknowledgment
8 bit data: The 8 data bits being transacted
P: I^{2}C STOP condition

This design example configures the iCE FPGA as an I^{2}C Slave. This I^{2}C Slave functions as a port expander via the I^{2}C bus, enabling the host system to effectively have multiple (up to 16, 8 input and 8 output) IO ports using just 2 ports (the I^{2}C's SDA and SCL ports).

Implementation

Fig 4 below illustrates the I^{2}C Slave port expander arrangement. The I^{2}C Master resides in the host system. The Slave is implemented in the iCE FPGA. The Slave has 8 input ports and 8 output ports. The port expander enables the Master to write upto 8 bits at a time through the Slave's output ports or read up to 8 bits through the Slave's input ports. For a demo, these inputs may be simulated by a keypad arrangement and output ports can be connected to an array of 8 LEDs to illustrate the conditions of the expanded 8 output ports.

Upon receiving the correct Slave address on the SDA line, the Slave duly acknowledges by pulling the SDA line low for single SCL clock high duration. If the Master had requested a READ operation (signified by an appended '1' bit to the 7 bit Slave address), the Slave will serially send the 8 individual bits set on its input ports on to the SDA line. If the Master had requested a WRITE operation (signified by the appended '0' bit to the 7 bit Slave address), the Slave will register the 8 bits it receives on the SDA line from the Master and then subsequently present them on its 8 output ports. Data exchanges between the Master and the Slave happen at the SCL clock rate. Slave detects Start and Stop conditions on the I^{2}C bus based on falling edge and rising edge of SDA line.

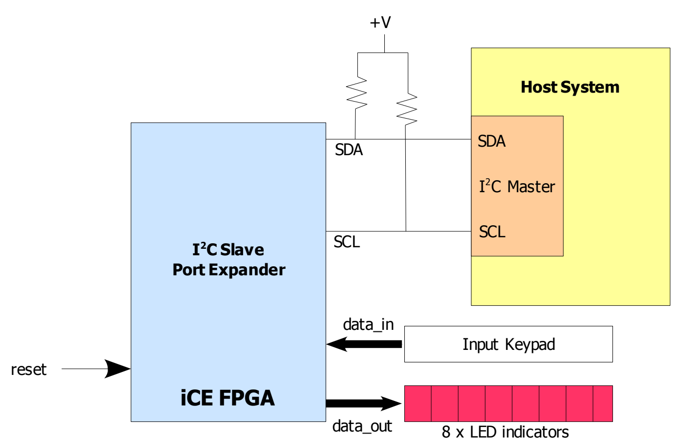

Fig 4: I^{2}C Slave implementation

Port	Direction	Description
reset	Input	Active low system reset
SDA	Inout	Open Drain type I^2C serial data line
SCL	Input	Open Drain type I^2C serial clock line
data_out[7:0]	Output	8 bit wide expanded data output port
data_in[7:0]	Input	8 bit wide expanded data input port

Table 1: Pin Description

Table 2 shows the post P&R resource utilization summary of this design when implemented using iCE FPGA.

Device	Logic Cells	IO Cells
iCE65L04-UCB284	77	19

Table 2: Resource Utilization

Conclusion

This design example demonstrates the implementation of an I^2C Slave performing port expansion on iCE FPGAs. The benefits of such a port expander towards reduction in pin count on the host system, thereby enabling smaller packaging, and I^2C's intrinsic pin count and board real estate saving characteristics are well complemented by iCE FPGA's very low power capabilities. This makes iCE FPGAs an obvious choice for I^2C Slave systems implementations, such as port expanders, in the context of all low power, battery operated and compact applications.

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