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DE REF #307

iCE65 as LCD CONTROLLER

Overview

This design example illustrates the implementation of a LCD Controller using iCE65 FPGAs. The implementation is for a standard 16 characters x2 line LCD display.

Description

LCD, or liquid crystal displays have increasingly become the most preferred display devices in most systems that require an user display. Their low power requirements, fast operation, low cost, and versatile features make them indispensable. LCD modules today have inbuilt in them the basic low level drivers, and most other support sub systems that are required to make them work. However a system interface, that caters to initialization and data preparation in accordance to the LCD's timing requirement is still required to be implemented. This design example is one such implementation wherein the LCD Controller has to perform operations like initialization of the display module and write valid data to the LCD's data lines after appropriately interfacing with the system's host unit. It waits on the user generated signals to control subsequent operations and generate necessary signals required by the LCD module.

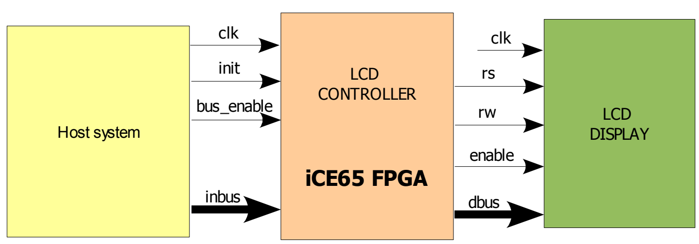

Fig 1: iCE65 FPGA as LCD Controller

Implementation

The LCD Controller is implemented using a finite state machine (FSM) architecture. Fig 2 in the following page indicates the sequence of events that are required to write a character to LCD. This FSM has the following important states:

- Start state
- Power Up state
- Initialization state
- LCD_write state

On reset, the FSM goes into Start state. Here it waits on inputs from the host system. The inputs the Start state monitors are **init** and **bus_enable**. Initially the host places a high on the **init** line for at least one clock cycle while **bus_enable** is held low. When the host does this, the state machine goes to the Power up state.
In the Power Up state the FSM waits for 15ms as required by the display. Once this is done it goes into the Initialization state. Here the FSM sends out a set of 7 commands to initialize the LCD display. The whole initialization process lasts for approximately 120 ms after which the FSM comes back to the Start state.
The host can now go for a Write operation or another initialization sequence as required. If the host chooses to go to perform a Write operation on the display, it places a high on the **bus_enable** line while holding the **init** pin low. **bus_enable** should be held high for at least one clock cycle and should be made low before 20 clock cycles. In the LCD_write state, the host places appropriate data on the **inbus.** This is then clocked into the LCD on the falling edge of the **enable** signal which is generated by the LCD_write state. The whole write operation takes 20 clock cycles at a frequency of 32.67khz.
Once the LCD_write state is complete, the FSM returns back to the Start state. The host can again go the write state by placing a high on the **bus_enable** line.

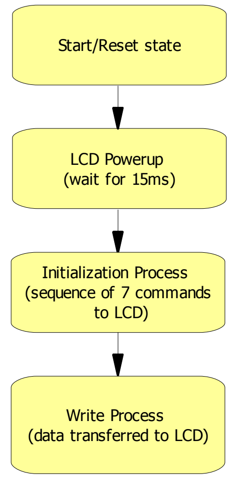

Fig 2: LCD controller sequence diagram

Port	Direction	Description
clk	Input	System clock
init	Input	Used for initializing the LCD display
Inbus[9:0]	Input	10 bit wide data corresponding to the information being sent to the LCD display
bus_enable	Input	Used to indicate data ready for a Write
Dbus[7:0]	Output	8 bit wide bus corresponding to the data written to the LCD display
rw	Output	Indicates Read/Write operation. A '0' specifies a Write. (This controller is restricted to only perform Write)
rs	Output	Indicates if the data on dbus is Write data (1) or a LCD instruction (0)
enable	Output	Enable signal - Generated by the LCD controller requesting to latch data into the LCD module at a falling edge

Table 1: Pin Description

Table 1 above indicates the various ports on the LCD controller. Table 2 below shows the post P&R resource utilization summary of this design when implemented on an iCE65 FPGA.

Device	Logic Cells	IO Cells
iCE65L04-UCB284	156	25

Table 2: Resource Utilization

Conclusion

This design example demonstrates the implementation of a LCD controller on iCE FPGAs. The low power properties of LCDs are well complemented by iCE FPGA's very low power capabilities. This makes iCE FPGAs an obvious choice for LCD controller applications in all low power, battery operated and compact applications.

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