

## PULSE WIDTH MODULATION

### Overview

Pulse width modulation(PWM) of a signal involves modulation of its duty cycle, to convey either information over a communication channel or control the amount of power sent to a load. PWM is employed in handhelds, portable systems, and low-power battery powered applications. This document provides a brief description of PWM and its implementation in SiliconBlue FPGAs.

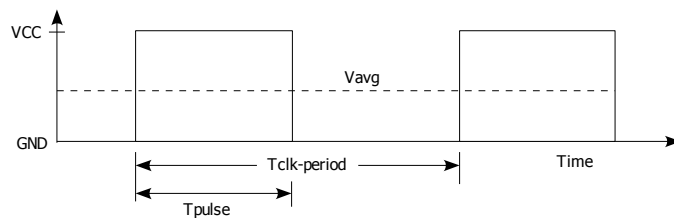
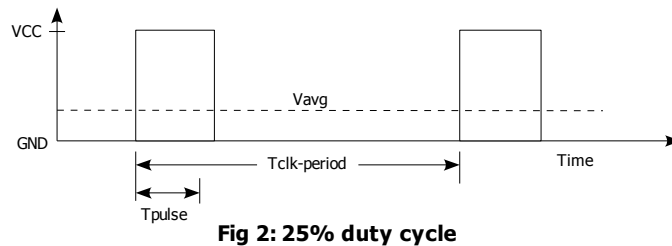
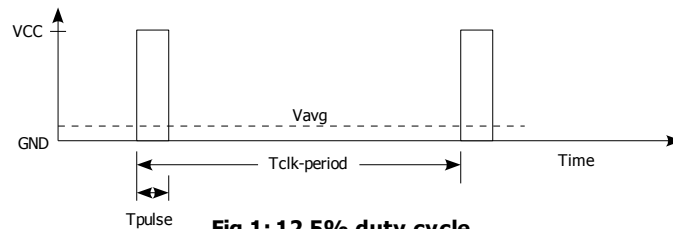
### Description

An analog signal has continuously varying value, with infinite resolution both in time and magnitude. Analog signals are distinguishable from digital signals because the latter always takes values only from a finite set  $\{+5V(VCC), 0V(GND)\}$ . PWM is one way of digitally encoding analog signal levels by averaging voltage over time. Through the use of high resolution counters, the duty cycle of a square wave is modulated to encode a specific analog voltage or current level. Duty cycle refers to the amount of time in the period that the pulse is high, which is typically specified as a percentage of the pulse period.

$$\text{Duty cycle} = (\text{Tpulse} / \text{Tclk-period}) * 100 \%$$

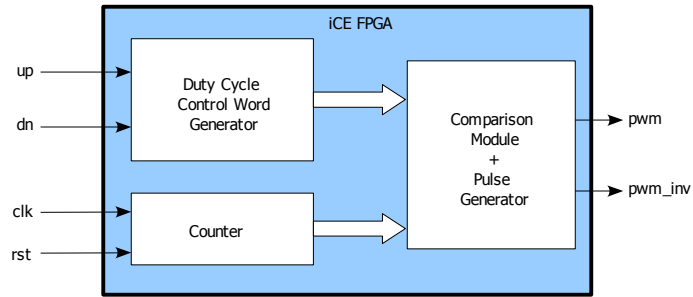
$$\text{Average Voltage} = \text{Duty cycle} * \text{Vcc}$$

For 12.5%, 25% and 50% duty cycle PWM, average analog voltage is 0.675, 1.25 and 2.5V respectively. Fig 1, 2 and 3 below shows 12.5%, 25% and 50% duty cycle PWM along with their associated average voltage.



# Implementation

Fig 4 below shows the basic block diagram of a PWM implementation. The 'up' and 'dn' signals control the duty cycle of PWM output. Table 1 describes the PWM user interfaces.



**Fig 4: Block diagram of PWM**

Port	Direction	Description
clk	In	PWM system Clock. PWM counter and Pulse generator operates at this frequency
up	In	Duty cycle of PWM pulse increases if this pin held high. 'up' pin has higher priority than 'dn' pin
dn	In	Duty cycle of PWM pulse decreases if this pin held high.
pwm	Out	PWM pulse output, whose duty cycle controlled by up/dn ports.
pwm_inv	Out	Inverted PWM pulse output.

**Table 1: PWM user interface description**

The PWM circuit functions as follows:

- Resets all registers to "00...00" when 'rst' pin is held high for about one clock cycle. This also resets PWM output port to high
- The counter module starts counting from "00...00" to "11...11"
- A high on the 'up' pin increments the duty cycle control word, where as a high on 'dn' pin decreases the duty cycle control word
- When duty cycle control word equals the counter count value, the PWM pulse goes low. PWM pulse goes high when counter starts at zero
- For every high on the 'up' pin, the duty cycle control word keeps increasing until it reaches the limit "11...11". At this point PWM pulse is of 100% duty cycle.
- For every high on 'dn' pin, the duty cycle control word keeps on decreasing until it reaches the lower limit "00...00". At this point PWM pulse is of 0% duty cycle.

Table 2 shows the resource utilization summary of this design when implemented using iCE FPGA.

Device	Logic Cells	IO Cells
iCE65L04-UCB284	64	6

**Table 2: Resource Utilization**

# Conclusion

This example design demonstrates the implementation of Pulse Width Modulation on iCE FPGAs. iCE FPGAs, due to their very low power capabilities, are ideal for implementing PWM applications used in the contexts of handheld and mobile devices where power saving is of paramount importance.

# Disclaimer

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