

Description

This device consists of four UART ports, eight level shifters and 16 general purpose outputs with an SPI bus interface. A microcontroller can communicate with UART peripherals and drive the 16 output ports through the SPI serial bus. A block diagram is shown in Figure 1.

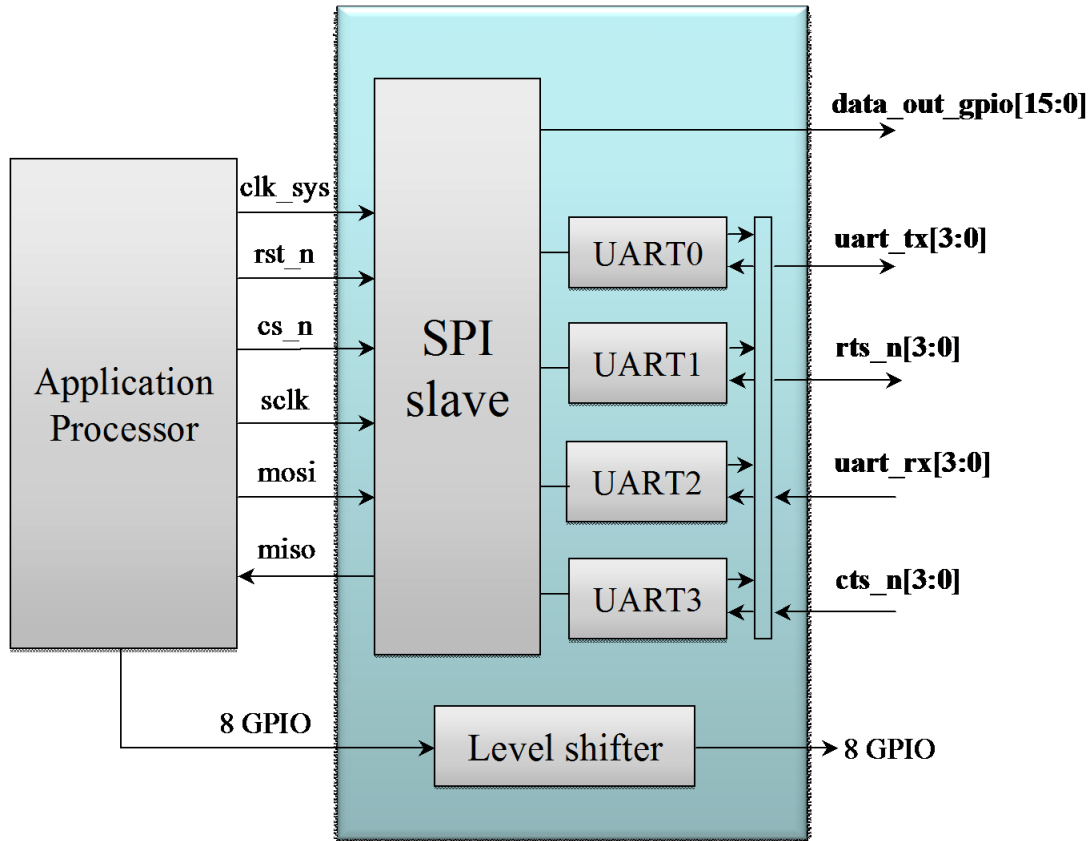


Figure 1: Design Block Diagram

Features

- SPI Slave operates in CPOL=0 and CPHA=0 mode
- SPI to GPIO port expansion
- SPI to UART expander
- 16 I/O port for the SPI bus
- 4 UART transceiver for the SPI bus
- Compatible with most microcontrollers
- 1.8V to 3.3V voltage level-translation
- 8 I/O port pair for voltage level-translation

SPI to UARTs with Voltage Level Translation and GPIO

Pin Description

Pin	Direction	Description
clk_sys	Input	System clock
rst_n	Input	System reset, active low
cs_n	Input	Chip select, active low
sclk	Input	SPI interface clock
mosi	Input	SPI serial data from master to slave
miso	Output	SPI serial data from slave to master
data_out_GPIO(15:0)	Output	16-bit output expansion port
uart_tx(3:0)	Output	UART transmit data
uart_rx(3:0)	Input	UART receive data
rts_n(3:0)	Output	nRTS, active low
cts_n(3:0)	Input	nCTS, active low
level_shift_in(7:0)	Input	8-bit level shift input port
level_shift_out(7:0)	Output	8-bit level shift output port

SPI to GPIO operation

There is the SPI MOSI frame structure for GPIO expander:

DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
FUNC=0	A3	A2	A1	A0	X	X	X	D	D	D	D	D	D	D	D

The DIN15 is the function control bit. When DIN15(FUNC) = 0, the follow 4 bits (A3,A2,A1,A0) are the address bits of the data_out_gpio ports. From DIN7 to DIN0 bits in the frame are the data to output ports. The data_out_gpio port that selected by address bits will output the 8 bits data that stored in the SPI frame from DIN7 to DIN0 serially.

The data on MISO line is not the valid data when the SPI MOSI frame is the GPIO frame. SPI master should discard the data on the MISO line in this situation.

SPI to UART expander operation

There are the SPI frames for SPI_UART expander:

DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
FUNC=1	X	X	A1	A0	M1	M0	X	X	PT	PE	L1	L0	B2	B1	B0

MOSI Frame – Config Write (MIM0 = 11)

DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
FUNC=1	X	X	A1	A0	M1	M0	X	D7	D6	D5	D4	D3	D2	D1	D0

MOSI Frame – Data Write (MIM0 = 10)

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
X	X	X	X	X	X	PER	BER	D7	D6	D5	D4	D3	D2	D1	D0

MISO Frame – Data Read (MIM0 = 00)

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
X	X	X	X	X	CTS	RTS	RXBSY	TXBSY	PER	BER	WFULL	REMPY	PE	L1	L0

MISO Frame – Status Read (MIM0 = 01)

MOSI Frame Configuration

Function Selection

Func	Description
1	UART Mode
0	GPIO Mode

Address Selection

A3,a2,A1,A0	Description
0000-1111	GPIO Address 0 - 15
xx00-xx11	UART Address 0 - 3

UART Mode

M1,M0	Description
00	reads UART register/FIFO
01	reads UART status register
10	writes UART register/FIFO
11	writes UART configuration register

Parity Control

Bits	Description
PE = 1	Enable Parity
PE = 0	Disable Parity
PT = 1	Odd Parity
PT = 0	Even Parity

Data Length

L1,L0	Description
00	5-bit
01	6-bit
10	7-bit
11	8-bit

Baud Rate (based on 4 MHz system clock frequency)

B2,B1,B0	Description
000	115.2K
001	57.6K
010	38.4K
011	19.2K
100	9600
101	4800
110	2400
111	1200

The last 8 bits in the MOSI frame contain the data byte to be written to the slave's output UART device. In read mode, the first 6 bits on the MISO data frame are invalid and are discarded. The following 10 bits contain the input data byte that the slave received on a selected UART port.

SPI to UARTs with Voltage Level Translation and GPIO

Level-Shift operation

The level shifter is the level translation block. The lower voltage I/O group will use pins in one I/O bank of the device, and the other voltage I/O group will use pins in another I/O bank of the device. These two I/O banks will support different I/O voltage standards. Also these two I/O groups can communicate each other.

Resource utilization

FFs	667
LUTs	1565
RAMs	8
IOBs	54

Revision History

Version	Date	Description
1.0	31-DEC-2008	Initial release.

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