March 2008
DE - 103

Port Expansion Using SPI bus Inteface

Introduction

This design example illustrates the capability of Silicon Blue's iCE65 to be used for I/O expansion as a SPI Slave. In many microprocessor based systems the number of pin counts are reduced to decrease the package size. This design example shows how to increase the GPIO pins via SPI interface protocol.

SPI Overview

SPI is a single Master multiple Slave protocol. It is a widely used four wire serial serial communication interface in embedded systems for interfacing microprocessor and various peripheral devices such as sensors, memory chips, port expanders, display drivers and data converters. The main advantage SPI interface has over other interface protocols such as the I2C is that SPI is a full duplex communication enabling higher throughput. The FPGA in this design example acts as a slave and uses following four (SPI) signals to interact with the SPI Master: MISO (Master in Slave out), MOSI (Master out Slave in), Clock and the Chip Select. Fig 1 illustrates the interface block digram and Table 1 provides the pin description.

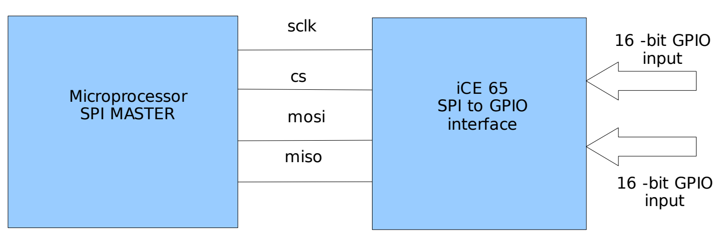

Fig 1. GPIO pin expansion via SPI interface

Port	Direction	Description
cs	In	Selection of the slave to be operated
sclk	In	Master controlled clock
miso	Out	Output pin for the slave, used by the master for reading purposes
mosi	In	Input pin for the slave, used by the master for writing purposes

Table 1. Pin Description of SPI slave

Implementation

The iCE65 presents sixteen general purpose input ports and sixteen general purpose output ports to the host. The host (Master) implementation communicates with the FPGA (slave) through the full duplex SPI interface. All the sixteen general purpose I/Os can hence be either read or written at the same time.

SPI interface
For the SPI interface, the FPGA (Slave) has an eight bit address register that controls the access to the 32 I/Os present. The first four bits (lower nibble) is addresses the input pins (Read operation). The last four bits (higher nibble) pertain to the output pins (Write operation). Figure 2. elaborates the frame format .

Address (input pins)	Address (output pins)	DATA (Bidirectional)
Lower nibble (Read)	**Higher nibble (Write)**	**Input from MOSI Output to MISO**

Fig 2. SPI frame format

GPIO Interface
The input and the output pins as addressed by the first byte are now active and read/write operation takes place only on these pins. For the next 8 clock cycles the data from the specific input pin is read and sent to the MISO line. The data from the MOSI is sent to specified output pin. Table 2 provides the GPIO expander's pin description

Port	Direction	Description
data_in	In	16-bit input pins for providing data for master to read
data_out	Out	16-bit output pins for writing the data sent by the master

Table 2. Pin Description for GPIO

The GPIO pin expansion application listed in this application when implemented using iCE device iCE65L04-UCB132C utilizes 29 filp flops and 78 LUTs .

Conclusion

This design example demonstrates the implementation of a GPIO pin expander as a SPI slave on an iCE FPGAs. iCE FPGAs due to their low power consumption property makes it an ideal choice for pin expansion on various microprocessors boards and embedded systems where power consumption is of chief importance.

Disclaimer