

## Voltage Level Translator

### Overview

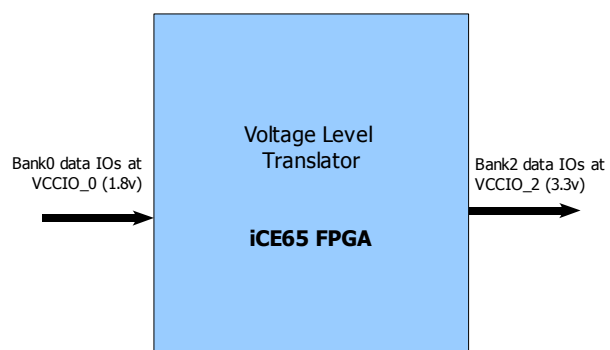
This design example explains the application of SiliconBlue iCE65 FPGA as a voltage level translator. The drive for lower power consumption has brought about the use of I/O standards that deal with low voltage logic and it is common practice to have various components in a design operate at different voltage levels. Popular I/O standards uses voltage levels like 1.5V, 1.8V, 2.5V and 3.3V. Thus a component working at a lower voltage level might have to communicate with a component working at higher voltage level. To enable compatibility between such components, the SiliconBlue iCE65 FPGA could be used as a bridging device.

### Description

The SiliconBlue's iCE65 FPGA architecture has four independent I/O Banks, each with its own voltage supply input, VCCIO\_x, which defines the I/O standard of that bank. Each of these I/O Banks can be configured independently of the other to support different voltage levels and there by facilitates voltage level translation.

In the example shown below (Fig 1), the Silicon Blue iCE65 functions as a voltage level translator for one set of ports at voltage level 1.8V to another set of ports at 3.3V.

Of the various voltages supported by the different I/O Banks, Banks 0, 1, 2 support 1.8V, 2.5V, 3.3V, while I/O Bank 3 can support 1.5V, 1.8V, 2.5V. I/O Bank 3 has additional I/O capabilities to support DDR, DDR2 and Mobile DDR SDRAM memory components.



**Fig 1: Voltage Level Translation**

## Description (contd.)

SPI Bus interface pins on iCE65 FPGA can be used as general purpose I/O pins to provide an optional fifth I/O Bank, with the SPI\_VCC specifying the voltage level.

### Supported I/O Standards:

1. LVCMOS at 2.5V, 1.8V, or 1.5V, controlled by the VCCIO\_3 input supply.
2. SSTL18 when VCCIO\_3 is 1.8V.
  - a. Class I
  - b. Class II
3. SSTL2 when VCCIO\_3 is 2.5V.
4. Mobile DDR when VCCIO\_3 is 1.8V.
5. LVDS Differential I/O when VCCIO\_3 is 2.5V.

### Input Pull-Up Resistors

The programmable IO pins along the top, right, and bottom edges (I/O Banks 0, 1, and 2) have an optional input pull-up resistor. This pull-up resistor is not provided in I/O Bank 3. The pull-up resistor is useful to tie off unused PIO pins, to prevent unwanted power consumption and possible damage to the chip. The SiliconBlue development software defines all unused PIO pins as inputs with the pull-up resistor turned on. Tables 1 and 2 give specifications on the supported I/O standards and voltage levels.

I/O Bank	Position at Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	N/A
1	Right	VCCIO_1	Yes	Yes	Yes	N/A
2	Bottom	VCCIO_2	Yes	Yes	Yes	N/A
3	Left	VCCIO_3	N/A	Yes	Yes	Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	N/A

**Table 1: Voltages supported by the respective I/O Banks**

I/O Standard	Supply Voltage	Drive Current (mA)	I/O Bank 0, I/O Bank 1, I/O Bank 2, SPI Interface	I/O Bank3
5V Input Tolerance	3.3V	N/A	Yes	N/A
LVCMOS33	3.3V		Yes	N/A
LVCMOS25	2.5V	+/- 10	-	Yes
		+/- 8	-	Yes
		+/- 6	Yes	-
		+/- 4	-	Yes
		+/- 2	-	Yes
LVCMOS18	1.8V	+/- 8	-	Yes
		+/- 4	Yes	Yes
		+/- 2	-	Yes
LVCMOS15	1.5V	+/- 3	N/A	Yes
SSTL2_II	2.5V	+/- 16.2	N/A	Yes
SSTL2_I	2.5V	+/- 8.1	N/A	Yes
SSTL18_II	1.8V	+/- 16.2	N/A	Yes
SSTL18_I	1.8V	+/- 8.1	N/A	Yes
MDDR	1.8V		N/A	Yes
LVDS	2.5V		N/A	Yes

**Table 2: I/O Standards supported by each I/O Bank**

## Implementation

The voltage level translator in this design is implemented as an 8-bit input and 8-bit output port.

When implementing this design, the only constraint to be noted is that the input as well as output pins be assigned to different I/O Banks, whose VCCIO\_# is appropriately assigned to required voltage levels to enable suitable voltage level translation.

The voltage level translator design listed in this application note does not use any Logic Cells. An 8-bit Voltage level translator uses 16 I/O Cells.

## Conclusion

This example design demonstrates the implementation of a voltage level translator on iCE FPGAs. iCE FPGAs, due to the availability of 4 I/O Banks operating at different voltage levels are useful for operating part of the design at lower voltages there by reducing overall power consumption.

## Disclaimer

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