

Overview

This design example illustrates the implementation of CF plus interface using SiliconBlue ultra low power iCE65L04 FPGA. Compact Flash(CF) is a mass storage device format used in portable electronic devices like digital cameras, PDAs and Cellular phones. For storage, Compact Flash typically uses flash memory in a standardized enclosure.

Features

- Supports PC Card ATA using IO
- Supports PC Card ATA using memory
- IP-XACT version 1.2 compliant

Resource Utilization

Table 1: Resource Utilization

LUTs	Registers	Memory	GBs	I/Os
55	19	0	0	0

Note: Resource Utilization is based on iCECube 2010.12.14671

System Block Diagram

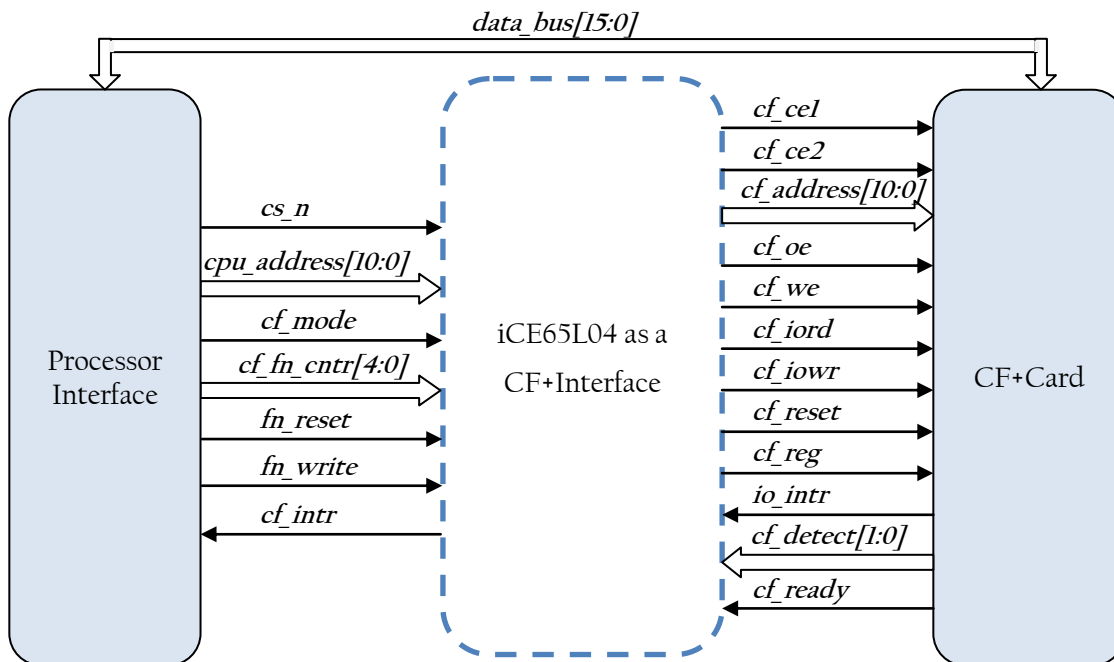


Figure 1: System Block Diagram

Functional Block Diagram

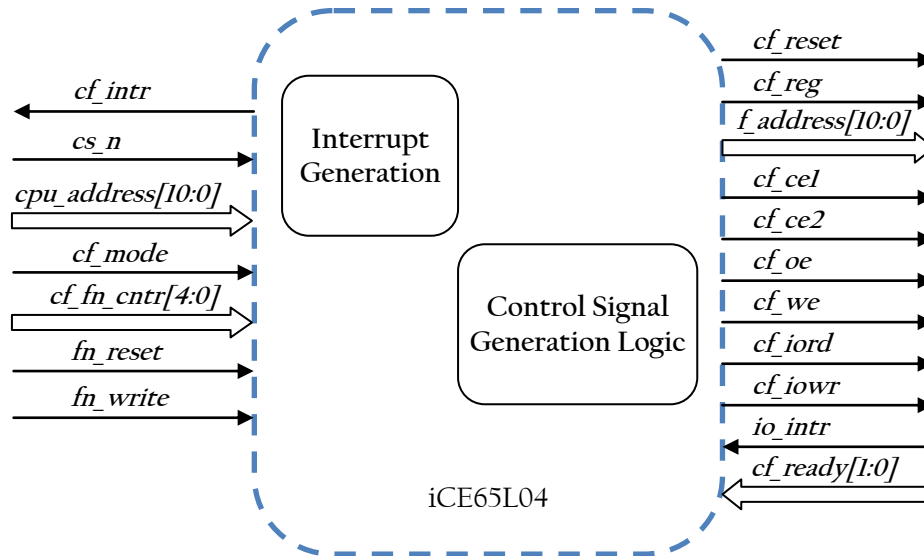


Figure 2: Functional Block Diagram

Design Interface

Table 1: Pin Description

Signal Name	Pin Type	Signal Description
cpu_address[10:0]	Input	Address Bus from Host.
cf_mode	Input	Selection lines to choose between I/O and memory mode operations.
cf_fn_cntrl[4:0]	Input	Selection lines to choose between I/O and memory R/W operations.
fn_reset	Input	Asynchronous active low reset pin asserted by host.
fn_write	Input	Rising edge generates control signals based on cf_fn_cntrl
cf_intr	Output	Interrupt line to the host, Active low for card detect.
cf_ready	Input	Asserted low during power up or reset, and made high in the memory mode
cf_detect[1:0]	Input	Active low Card detect signals
io_intr	Input	Interrupt request from I/O Device
cs_n	Input	Active low chip Select
cf_reg	Output	Low during I/O operations, used in memory mode
cf_reset	Output	Compact flash reset pin, Active High.
cf_iowr	Output	Active low I/O write select line
cf_iord	Output	Active low I/O read select line
cf_we	Output	Active low write enable line used to write to configuration registers
cf_oe	Output	Active low output enable line
cf_address[10:0]	Output	Address Bus
cf_ce1	Output	Active low card select signal
cf_ce2	Output	Active low card select signal

Configurable Parameters

None

Register Map

This design does not have any user accessible registers or memory.

Design Details

Interrupt Generation : An interrupt is generated and communicated to the host processor on the cf_intr line when a valid card insertion is detected.

Control Signal Generation Logic : The CF+ interface design monitors host side transaction requests to the CF+ card or the I/O card. Depending on the host processor request, the appropriate control signals are sent to the CF+ along with the address. The sequence of operation is as follows:

- Host processor pulls cs_n low and enables the CF+ card interface
- The pins cf_detect[1:0] goes low when CompactFlash card inserted into the socket
- CF+ Interface generates a low on cf_intr and communicates to the host processor that CF+ Interface is now activated
- Host generates a high on fn_write indicating to the Interface that the host is ready for data transaction
- All the transactions of the interface, CF+ card and host processor are synchronized with the fn_write signal.

On the rising edge of the `fn_write`, the FSM samples `cf_fn_cntrl[4:0]` pins. Each operation in both the modes is encoded with 5 bits specified by the controller using the `cf_fn_cntrl` pins. The FSM on every rising edge of `fn_write` decodes the `cf_fn_cntrl` line and generates the necessary control signals to carry out the requested operation successfully. The control signals generated by the interface during memory operation are `cf_we` and `cf_oe`, while during I/O operations the control signals generated are `cf_iord` and `cf_iowr`. The other control signals generated by CF+ Interface are CF enable signals, `cf_ce1` and `cf_ce2`, and memory enable signal `cf_reg`, are common for both modes. The logic levels of these generated signals are defined as per the CF+ standard.

The host data bus [15:0] and card data bus[15:0] are connected to each other without going through the FPGA.

The `fn_reset` signal is generated by the host. When receiving this, iCE65 generates the reset signal to the CF+ card. The `fn_reset` triggers a high on `cf_reset`(hardware reset) as well as the control signals necessary to configure the configuration registers for CF+ reset functionality..

System Designer Flow

CF+ Interface is compatible with System Designer/IP-XACT 1.2. The System Designer flow is as follows,

1. Launch the System Designer from Synplify Pro using menu 'Import -> Launch System Designer'.
2. Create a new project(open an existing old project, as necessary) and import the IP-XACT XML file
3. Drag and place the component from the 'Library' pane to the 'Design' pane
4. Click on the “Generate Files” button, which generates the necessary files required for synthesis and simulation.
5. Go to Synplify Pro and click on the “Run” button to synthesize the System Designer generated files. Synplify Pro generates all the necessary files for P&R in iCECube2.

References

The following references were used in the creation of this design:

- SiliconBlue Technologies, Inc. "[iCE65 Ultra Low-Power mobileFPGA Family](#)" datasheet (26-May-2010).
- www.compactflash.org

Revision History

Version	Date	Description
1.0	09-SEP-2010	Initial Draft Document
1.1	07-DEC-2010	IP-XACT format Update

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