

Overview

The LCD (Liquid Crystal Display) is currently among the most widely used devices to view images and videos. They can be seen in many applications, ranging from cell phones to televisions. This document provides a brief description of LCD Controller and its implementation on SiliconBlue FPGAs.

Features

- Configurable image resolutions (maximum of 1280 x 800)
- Configurable Front and Back Porches for both VSYNC and HSYNC signals
- Configurable VSYNC and HSYNC Pulse widths and polarities
- IP-XACT version 1.2 compliant

Resource Utilization

Table 1: Resource Utilization

LUTs	Registers	Memory	GBs	I/Os
206	160	0	0	0

Note: Resource Utilization is based on iCECube 2010.12.14856 release.

System Block Diagram

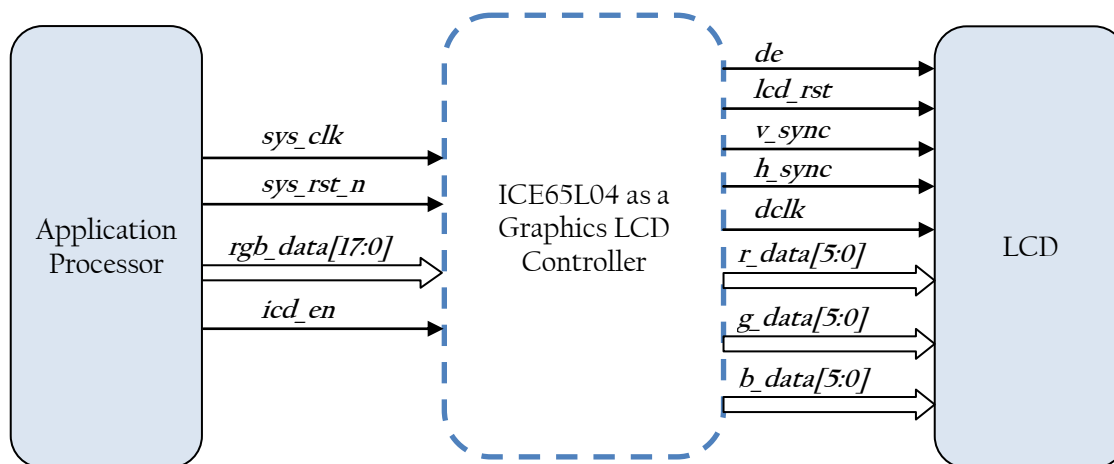


Figure 1: System Block Diagram

Functional Block Diagram

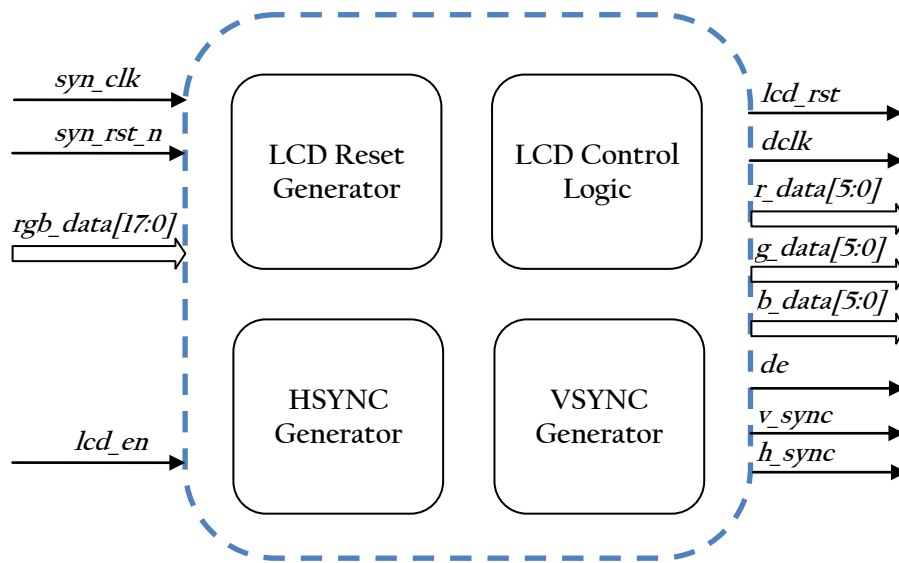


Figure 2: Functional Block Diagram

Design Interface

Table 2: Pin Description

Signal Name	Pin Type	Signal Description
sys_clk	Input	System clock
sys_rst_n	Input	Asynchronous Active Low System Reset
lcd_en	Input	Enable signal to the LCD Controller
rgb_data[0]	Input	RGB Data
rgb_data[1]	Input	RGB Data
rgb_data[2]	Input	RGB Data
rgb_data[3]	Input	RGB Data
rgb_data[4]	Input	RGB Data
rgb_data[5]	Input	RGB Data
rgb_data[6]	Input	RGB Data
rgb_data[7]	Input	RGB Data
rgb_data[8]	Input	RGB Data
rgb_data[9]	Input	RGB Data
rgb_data[10]	Input	RGB Data
rgb_data[11]	Input	RGB Data
rgb_data[12]	Input	RGB Data
rgb_data[13]	Input	RGB Data
rgb_data[14]	Input	RGB Data
rgb_data[15]	Input	RGB Data
rgb_data[16]	Input	RGB Data
rgb_data[17]	Input	RGB Data
v_sync	Output	VSYNC signal to the LCD
h_sync	Output	HSYNC signal to the LCD
de	Output	DE signal to the LCD
dclk	Output	DCLK signal to the LCD
lcd_rst	Output	Reset signal to the LCD
r_data[0]	Output	Red Component Data to the LCD
r_data[1]	Output	Red Component Data to the LCD
r_data[2]	Output	Red Component Data to the LCD
r_data[3]	Output	Red Component Data to the LCD
r_data[4]	Output	Red Component Data to the LCD
r_data[5]	Output	Red Component Data to the LCD
g_data[0]	Output	Green Component Data to the LCD
g_data[1]	Output	Green Component Data to the LCD
g_data[2]	Output	Green Component Data to the LCD
g_data[3]	Output	Green Component Data to the LCD
g_data[4]	Output	Green Component Data to the LCD
g_data[5]	Output	Green Component Data to the LCD
b_data[0]	Output	Blue Component Data to the LCD
b_data[1]	Output	Blue Component Data to the LCD
b_data[2]	Output	Blue Component Data to the LCD
b_data[3]	Output	Blue Component Data to the LCD
b_data[4]	Output	Blue Component Data to the LCD
b_data[5]	Output	Blue Component Data to the LCD

Configurable Parameters

- **V_SYNC_BACK_PORCH** : This is the distance between the top of the display to the upper most portion of the actual image. Its default value is 20. This can be modified as per the LCD used
- **V_SYNC_FRONT_PORCH** : This is the distance between the bottom of the display to the lower most portion of the actual image. Its default value is 28. This can be modified as per the LCD used
- **V_SYNC_ACTIVE** : The height of the actual image. Its default value is 1280.
- **V_SYNC_PULSE_WIDTH** : This is used to signify the beginning of a new frame. Its default value is 2. This can be modified as per the LCD used
- **V_SYNC_POL** : This is the polarity of the VSYNC signal. It can be active high (1) or active low (0). This can be modified as per the LCD used
- **H_SYNC_BACK_PORCH** : This is the distance between the left part of the display to the left most portion of the actual image. Its default value is 40. This can be modified as per the LCD used
- **H_SYNC_FRONT_PORCH** : This is the distance between the right part of the display to the right most portion of the actual image. Its default value is 24. This can be modified as per the LCD used
- **H_SYNC_ACTIVE** : The width of the actual image. Its default value is 800.
- **H_SYNC_PULSE_WIDTH** : This is used to signify the beginning of a new line in the frame. Its default value is 6. This can be modified as per the LCD used
- **H_SYNC_POL** : This is the polarity of the HSYNC signal. It can be active high (1) or active low (0). This can be modified as per the LCD used

Design Details

HSYNC Generator : Generates the HSYNC signal to the LCD based on a 11-bit pixel counter, which keeps track of the active and dummy pixels per frame. It also depends on the HSYNC pulse width, HSYNC back and front porch and the image width.

VSYNC Generator : Generates the VSYNC signal to the LCD based on a 11-bit line counter, which keeps track of the active and dummy lines per frame. It also depends on the VSYNC pulse width, VSYNC back porch and the image height.

LCD Control Logic : Generates the DE signal as well as the RGB data to the LCD. The data coming out of the Graphics LCD Controller is valid only when DE is high.

LCD Reset Generator : Generates the LCD Reset signal. The polarity of the Reset signal can be configured in the package. The Reset signal is generated after 1 ms.

Timing Diagrams

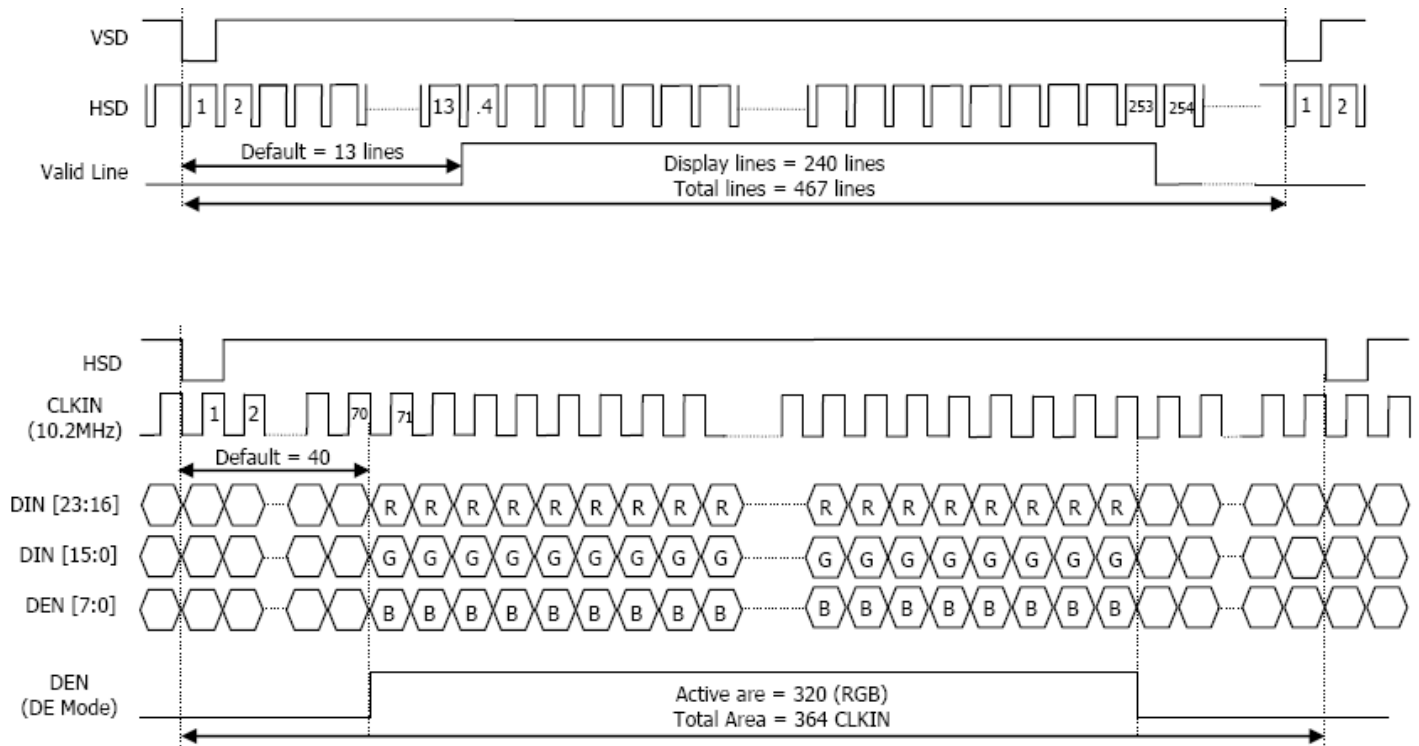


Figure 3: Timing Diagram of a 320 x 240 Graphics LCD Controller

System Designer Flow

Graphics LCD Controller is compatible with System Designer/IP-XACT 1.2. Following parameters can be configured in the System Designer environment,

- V_SYNC_BACK_PORCH – Default value is 20
- V_SYNC_FRONT_PORCH – Default value is 28
- V_SYNC_ACTIVE – The actual image height. Default value is 1280
- V_SYNC_PULSE_WIDTH – Default value is 2
- V_SYNC_POL – VSYNC signal polarity. Supports values 0 (active low) and 1 (active high), 0 being the default value
- H_SYNC_BACK_PORCH – Default value is 40
- H_SYNC_FRONT_PORCH – Default value is 24
- H_SYNC_ACTIVE – The actual image width. Default value is 800
- H_SYNC_PULSE_WIDTH – Default value is 6
- H_SYNC_POL – HSYNC signal polarity. Supports values 0 (active low) and 1 (active high), 0 being the default value

The System Designer flow is as follows,

1. Launch the System Designer from Synplify Pro using menu 'Import -> Launch System Designer'

2. Create a new project (open an existing old project, as necessary) and import the IP-XACT XML file
3. Drag and place the component from the 'Library' pane to the 'Design' pane. To change any parameters mentioned above, right-click the component instance and click on “Open Configuration”. Go to “Edit Instance Parameters” tab and change the parameters as required
4. Click on the “Generate Files” button, which generates the necessary files required for synthesis and simulation
5. Go to Synplify Pro and click on the “Run” button to synthesize the System Designer generated files. Synplify Pro generates all the necessary files for P&R in iCECube2

References

The following references were used in the creation of this design:

- SiliconBlue Technologies, Inc. "[iCE65 Ultra Low-Power mobileFPGA Family](#)" datasheet (26-May-2010).

Revision History

Version	Date	Description
1.0	09-SEP-2010	Initial Draft Document
1.1	21-DEC-2010	IP-XACT format Update

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