

Overview

Memory Stick is a removable flash memory card, which is used as storage media for the portable devices like digital cameras, digital music players, PDAs and cellular phones. This design example illustrates the implementation of a Memory Stick interface using an iCE65 FPGAs.

Features

- Parallel mode support
- Configurable clock frequency
- MS detect debounce logic
- Busy/Ready Interrupt generation
- Configurable data R/W size.
- IP-XACT version 1.2 compliant

Resource Utilization

Table 1: Resource Utilization

LUTs	Registers	Memory	GBs	I/Os
201	102	0	0	0

Note: Resource Utilization is based on iCECube 2010.12.14671

System Block Diagram

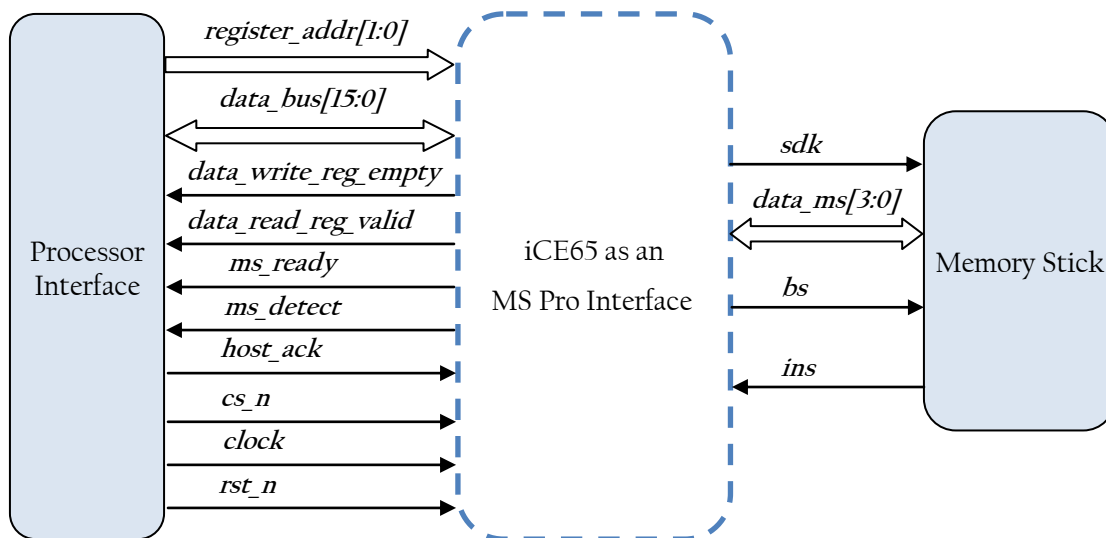


Figure 1: System Block Diagram

Functional Block Diagram

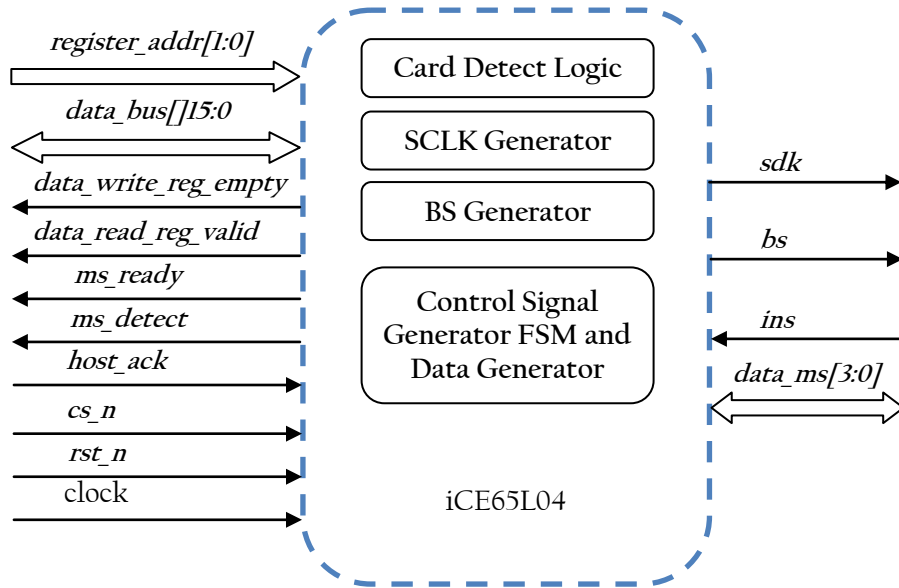


Figure 2: Functional Block Diagram

Design Interface

Table 1: Pin Description

Signal Name	Pin Type	Signal Description
cs_n	Input	Chip select signal generated by the host.
rst_n	Input	Asynchronous Active low system reset.
clock	Input	System clock.
data_bus[15:0]	Inout	Bidirectional data bus from Host Processor.
register_addr[1:0]	Input	Select line for data or command register operation.
data_read_reg_valid	Output	Goes high when data register is full. [For read operations]
data_write_reg_empty	Output	Goes high when data register is empty. [For write operations]
ms_detect	Output	Active high MS Card detection to Host processor.
host_ack	Input	Host sends a HIGH on this pin as soon as it acknowledges data_read_reg_valid or data_write_reg_empty signals. If not acknowledged, it suspends the communication by keeping sclk LOW.
sclk	Output	Clock signal generated which is 1/4th the system clock.
ins	Input	MS Pro Insertion/Removal detector. This pin goes low when MS Pro is inserted into the socket.
data_ms[3:0]	Inout	MS data bus
bs	Output	Bus State Signal. This signal operates in 4 modes. BS0 : Idle state. BS is held low. BS1 : TPC command Write state. BS held High. BS2 : BS held low. If data read operation, then BUSY/RDY status available on Data lines. If data write operation, then writes data on Data lines. BS3: BS Held High. If data write operation, then BUSY/RDY status available on Data lines. If data read operation, then data from MS Pro is available on Data lines

Configurable Parameters

None

Register Map

There are two user accessible registers within this design. They are the command register and the data write register. These are write only registers.

When chip select “cs_n” asserted low, then command/data read/write operations are executed as follows:

- when "00" – No operation. MS Pro Stick deselected.
- when "01" - Command Write to MS IF TPC Register
- when "10" - Data Read from MS IF Data Register
- when "11" - Data Write to MS IF Data Register

Data is read/written in MSB byte first format.

Command Write register : This is used to configure the operation between the Host Processor and the MS Pro Stick. The register layout is as follows :

Bits 15 - 1	Bit 11 - 10	Bit 9 - 0
TPC1	X	Number of bytes in transaction

This register can be accessed by pulling down the “cs_n” line with the register_addr line set to “01”.

When the command register is written, the communication protocol with the MS Pro device starts. The data transfer direction with the Memory Stick is determined from TPC[3]. When TPC[3] = 0, the read protocol is performed, otherwise the write protocol is performed. When the protocol starts, ms_ready changes to ‘0’ to indicate that protocol execution is underway. ms_ready held 0 throughout the communication with the Memory Stick, and generates an interrupt at the end of communication by sending a High on ms_ready pin. TPC Register[15:12] is the command part and TPC[9:0] provides the Transmit/Receive Data Size information to the MS Pro IF.

data write register : This is a 16-bit data register which contains the data to be transferred during a write transaction. This register is accessed by pulling down the cs line and the register_addr line set to “11”.

Design Details

Card Detect logic : Tells the host processor if a card has been inserted or removed from the MS Pro slot. This primarily uses the signal ins to determine the status.

SCLK Generator : SCLK is the clock at which the MS pro card is synchronized with. In this design the SCLK is 1/4th system clock frequency.

BS generator : The bus state signal operates in 4 modes which are :

BS0 : Idle state. BS is held low.

BS1 : TPC command Write state. BS held High.

BS2 : BS held low. If data read operation, then BUSY/RDY status available on Data lines. If data write operation, then writes data on Data lines.

BS3: BS Held High. If data write operation, then BUSY/RDY status available on Data lines. If data read operation, then data from MS Pro is available on Data lines.

This is generated by the BS generator module as required.

Control Signal Generation FSM and Data Generator : This generates the necessary control signals for the transaction with the MS Pro..

Timing Diagram

Figure 3 below shows the timing diagram for operations using the serial interface.

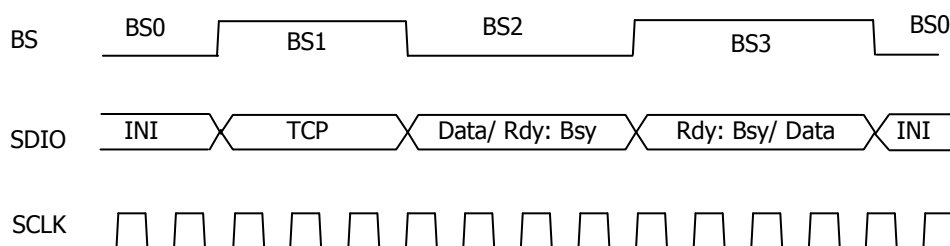


Figure 3: Operations using serial interface

Figure 4 below shows the timing diagram for operations using the parallel interface.

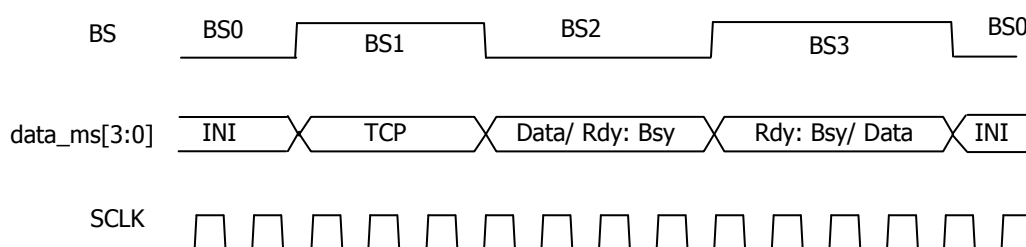


Figure 4: Operations using parallel interface

System Designer Flow

MS Pro Interface is compatible with System Designer/IP-XACT 1.2. The System Designer flow is as follows,

1. Launch the System Designer from Synplify Pro using menu 'Import -> Launch System Designer'.
2. Create a new project (open an existing old project, as necessary) and import the IP-XACT XML file
3. Drag and place the component from the 'Library' pane to the 'Design' pane
4. Click on the "Generate Files" button, which generates the necessary files required for synthesis and simulation.
5. Go to Synplify Pro and click on the "Run" button to synthesize the System Designer generated files. Synplify Pro generates all the necessary files for P&R in iCECube2.

References

The following references were used in the creation of this design:

- SiliconBlue Technologies, Inc. "[iCE65 Ultra Low-Power mobileFPGA Family](#)" datasheet (26-May-2010).

Revision History

Version	Date	Description
1.0	09-SEP-2010	Initial Draft Document
1.1	07-DEC-2010	IP-XACT format Update

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