iCE65 as a PWM Generator

Overview

Pulse Width Modulation (PWM) of a signal involves the modulation of its duty cycle, to convey either information over a communication channel or control the amount of power sent to a load. PWM is employed in a variety of applications, ranging from measurements and communications to power control and conversion, mainly because of its low power, noise-free and low cost characteristics. This document provides a brief description of PWM and its implementation on SiliconBlue FPGAs.

Features Supported

- User configurable PWM resolution
- Pulse Width Control using up/down signals
- Both direct and inverted PWM outputs
- VHDL RTL, testbench and ModelSim script for simulation
- IP-XACT version 1.2 compliant

Resource Utilization

Table 1: **Resource Utilization**

LUTs	Registers	Memory	GBs	I/Os
34	17	0	0	0

Note: Resource Utilization is based on iCEcube 2010.12.14671 release.

System Block Diagram

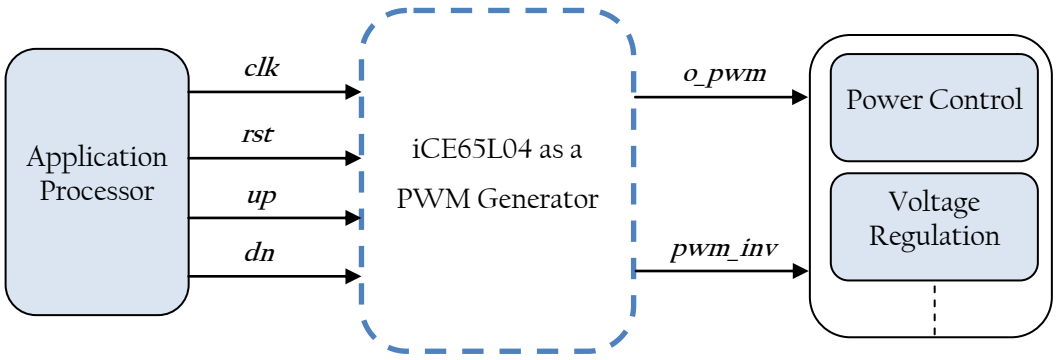

Figure 1: **System Block Diagram**

Functional Block Diagram

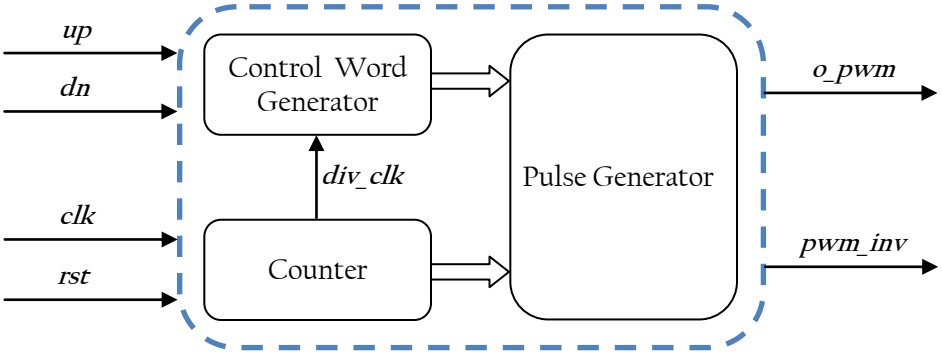

Figure 2: **Functional Block Diagram**

Design Interface

Table 1: **Pin Description**

Signal Name	Pin Type	Signal Description
clk	Input	System clock
rst	Input	Asynchronous active high system reset
up	Input	Increase in Duty cycle when held high. 'up' has higher priority than 'dn'
dn	Input	Decrease in Duty cycle when held high
o_pwm	Output	PWM signal
pwm_inv	Output	Inverted PWM signal

Configurable Parameters

- PWM_SIZE : This parameter configures the PWM resolution, which can be calculated as 1 / (2 ^ PWM_SIZE). The value of PWM_SIZE can range from 2 to 15, the default being 8.

Design Details

Control Word Generator : Generates a Control Word based on 'up' and 'dn' signals. Control word increases when 'up' is held high and decreases when 'dn' is held high. The Resolution (pwm_size) parameter controls the control word range.

Counter : This is a simple counter, cycles through counts 0 to maximum range, which is controlled by the generic parameter pwm_size.

Pulse Generator : This module compares the Counter and the Control Word Generator. Generates a High on PWM output until the Counter output reaches the Control word and Low afterwards.

Timing Diagram

Signals definition:

clk – System Clock

up – "up" signal to increase the duty cycle of the PWM signal

dn – "dn" signal to decrease the duty cycle of the PWM signal

o_pwm – Resultant PWM signal

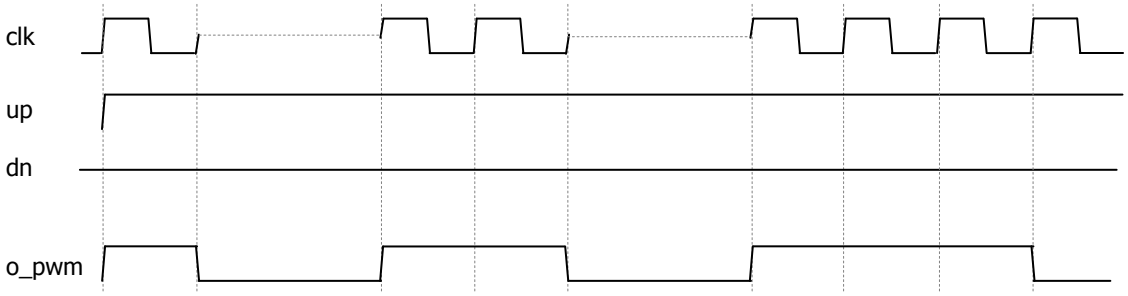

Figure 3: **Operations using serial interface**

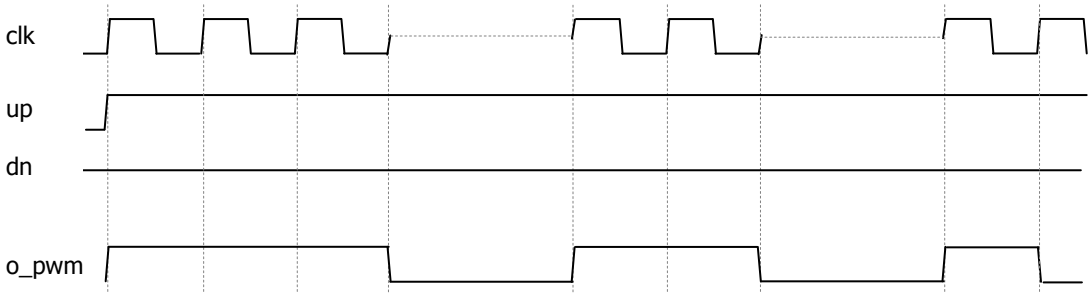

Figure 4: **Operations using parallel interface**

Usage Examples

Initialization Condition

When 'rst' is High, 'pwm' will be Low and 'pwm_inv' will be High.

Example #1

Keep 'up' High. The duty cycle of 'pwm' will keep increasing (shown in Figure 3), and the duty cycle of 'pwm_inv' will decrease.

(If both 'up' and 'dn' are high, 'up' will have higher priority than 'dn')

Example #2

Keep 'dn' High and 'up' low. The duty cycle of 'pwm' will keep decreasing (shown in Figure 4) and the duty cycle of 'pwm_inv' will increase.

System Designer Flow

PWM is compatible with System Designer/IP-XACT 1.2. Following parameter can be configured in the System Designer environment:

- PWM_SIZE – This parameter configures the PWM output resolution. Its default value is 8, minimum value is 2

The System Designer flow is as follows,

1. Launch the System Designer from Synplify Pro using menu 'Import -> Launch System Designer'.
2. Create a new project(open an existing old project, as necessary) and import the IP-XACT XML file
3. Drag and place the component from the 'Library' pane to the 'Design' pane
4. To change the PWM Resolution, right-click on the component instance, and click on "Open Configuration". Go to "Edit Instance Parameters" tab, change the "PWM_SIZE" parameter. Click on the "Apply" button, and then close it.
5. Click on the "Generate Files" button, which generates the necessary files required for synthesis and simulation.
6. Go to Synplify Pro and click on the "Run" button to synthesize the System Designer generated files. Synplify Pro generates all the necessary files for P&R in iCECube2.

References

The following references were used in the creation of this design:

- SiliconBlue Technologies, Inc. "iCE65 Ultra Low-Power mobileFPGA Family" datasheet (26-MAY-2010)..

Revision History

Version	Date	Description
1.0	09-SEP-2010	Initial Draft Document
1.1	03-DEC-2010	IP-XACT format Update

Disclaimer

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