

Overview

A touch screen is a display which can detect the location of touches within the display area. This design example demonstrates the use of SiliconBlue iCE FPGAs as a touch screen controller for use with low power hand held devices. It is also provided with an asynchronous processor interface.

Features

- Compatible with Digitizer chip(TSC2046)
- Touch Debounce logic
- 16x32 Touch Screen Resolution
- Interrupt generation logic
- IP-XACT version 1.2 compliant

Features not supported

- Power save mode support
- Configurable resolution
- Configurable for digitizer chips with SPI or I2C interfaces

Resource Utilization

Table 1: Resource Utilization

LUTs	Registers	Memory	I/Os	GBs
171	128	1	0	0

Note: Resource Utilization is based on iCECube2 2010.12.14671.

System Block Diagram

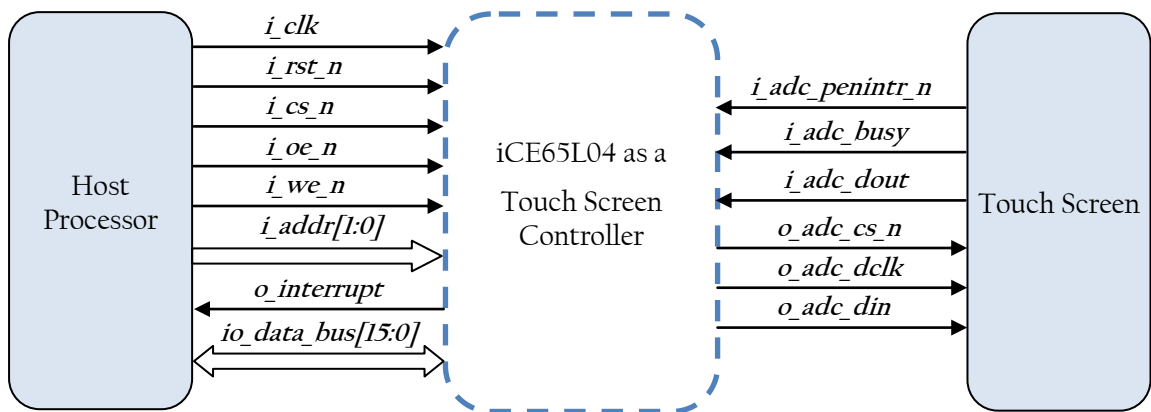


Figure 1: System Block Diagram

Functional Block Diagram

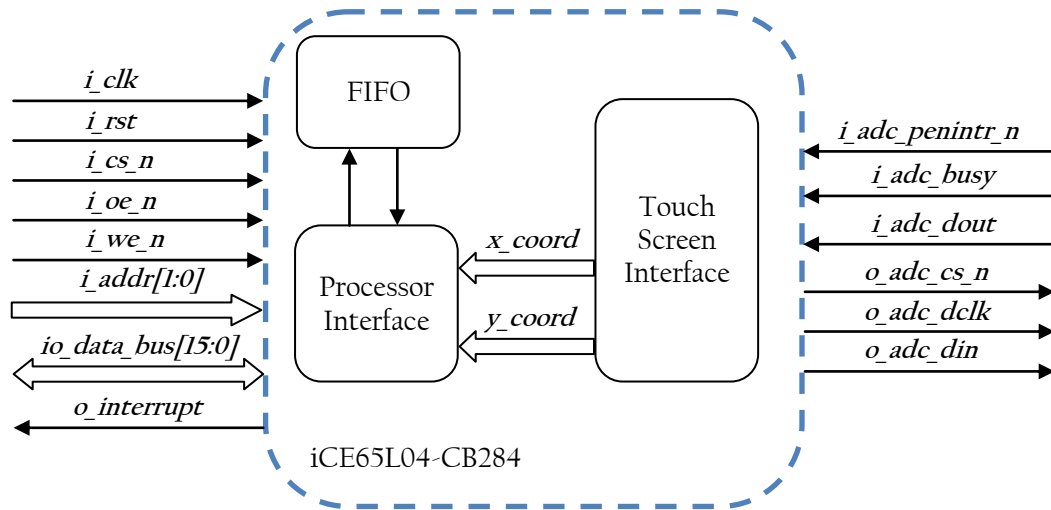


Figure 2: Functional Block Diagram

Design Interface

Table 1: Pin Description

Signal Name	Pin Type	Signal Description
i_clk	Input	System clock operating at 32MHz.
i_rst_n	Input	Asynchronous active low system reset.
i_adc_penintr_n	Input	Touch Screen Pen Interrupt
i_adc_busy	Input	Touch Screen Busy
o_adc_cs_n	Output	Touch Screen Chip Select
o_adc_dclk	Output	Touch Screen dot clk
i_adc_dout	Input	Touch Screen serial data out
o_adc_din	Output	Touch Screen serial data in
o_interrupt	Output	Interrupt Signal to host processor
io_data_bus[15:0]	Inout	Bidirectional processor data bus
i_cs_n	Input	Chip select
i_oe_n	Input	Output Enable
i_we_n	Input	Write Enable
i_addr[1:0]	Input	Address lines to access internal registers

Configurable Parameters

- **max_x** : This parameter configures the number of x co-ordinates to be used. The supported values include 8 and 16 (default).
- **max_y** : This parameter configures the number of y co-ordinates to be used. The supported values include 16 and 32 (default).

Register Map

Table 2 gives the address mapping and description for the registers used within this design. These registers are read only registers.

Table 2: Read only Register set of the Touch Screen Controller design

Address	Registers
00	Valid data register
01	FIFO Status register

Design Details

Touch Screen Interface : The touchscreen controller waits on the input signal, **i_adc_penintr_n**, to go low which indicates that a touch has taken place.

The interface logic then waits for the debounce time and starts to sample the x-coordinate and y-coordinate data. This data is passed onto the processor interface for storage.

Processor Interface : The following signals are used for transactions between the host processor and the touch screen interface – **i_cs_n**, **i_oe_n**, **i_we_n**, **i_addr**, **io_data_bus**. For all transactions to be valid the **i_cs** must be held low. Since the internal registers of this interface is read only, only the **i_oe_n** signal is used and the **i_we_n** is provided in scope of future enhancements.

The control signal for the read operation is output enable signal **i_oe_n**. The host processor can use this signal with the chip select line **i_cs_n** to read either the touch data within the RAM or the status of the FIFO.

As long as valid touch data is available within the RAM an Interrupt is generated by the touch screen interface module. The interrupt is de-asserted once all the valid data had been read from the RAM.

The touch data received by Processor interface block from the Touch Screen Interface block is stored in the FIFO.

FIFO : The FIFO is provided to store the processed touch data. The depth of this FIFO is 128 and stores 16 bit of data at each location.

Timing Diagram

Figure 3 below shows the timing diagram for the register read operation.

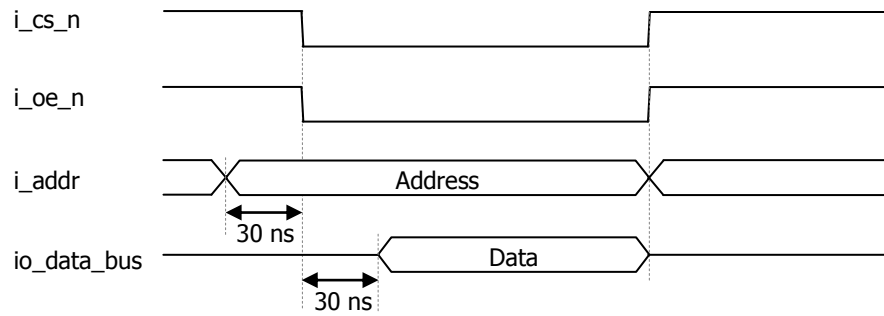


Figure 3: Timing diagram for the register read operation

System Designer Flow

Touch Screen Controller is compatible with System Designer/IP-XACT 1.2. Following parameters can be configured in the System Designer environment:

- `max_x` – This parameter configures the number of x co-ordinates to be used. The supported values are 8 and 16 (default).
- `max_y` – This parameter configures the number of y co-ordinates to be used. The supported values are 16 and 32 (default).

The System Designer flow is as follows,

1. Launch the System Designer from Synplify Pro using menu 'Import -> Launch System Designer'.
2. Create a new project (open an existing old project, as necessary) and import the IP-XACT XML file
3. Drag and place the component from the 'Library' pane to the 'Design' pane
4. To change the number of x co-ordinates and y co-ordinates, right-click on the component instance, and click on "Open Configuration". Go to "Edit Instance Parameters" tab, change the "max_x" and "max_y" parameter values as required. Click on the "Apply" button, and then close it.
5. Click on the "Generate Files" button, which generates the necessary files required for synthesis and simulation.
6. Go to Synplify Pro and click on the "Run" button to synthesize the System Designer generated files. Synplify Pro generates all the necessary files for P&R in iCECube2.

References

The following references were used in the creation of this design:

- SiliconBlue Technologies, Inc. "[iCE65 Ultra Low-Power mobileFPGA Family](#)" datasheet (26-May-2010).

Revision History

Version	Date	Description
1.0	09-SEP-2010	Initial Draft Document
1.1	08-DEC-2010	IP-XACT Format Update

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