iCE65 as YCbCr 10-bit To RGB888 Converter

Overview

YCbCr 10-bit to RGB888 converter converts YCbCr 4:2:0 10-bit color space information to RGB888 color space. To facilitate easy insertion to practical video systems, the design example takes up to three video stream control signals (H_SYNC, V_SYNC, FID, and DEN) and delays them appropriately, so that control signals can be easily synchronized with the output video stream.

Features

- 10-bit YCbCr 4:2:0 input and RGB888 output
- Pipelined implementation
- Latency of 4 cycles
- H_SYNC, V_SYNC, FID and DEN control signals for video synchronization
- VHDL RTL and functional test bench
- IP-XACT version 1.2 compliant

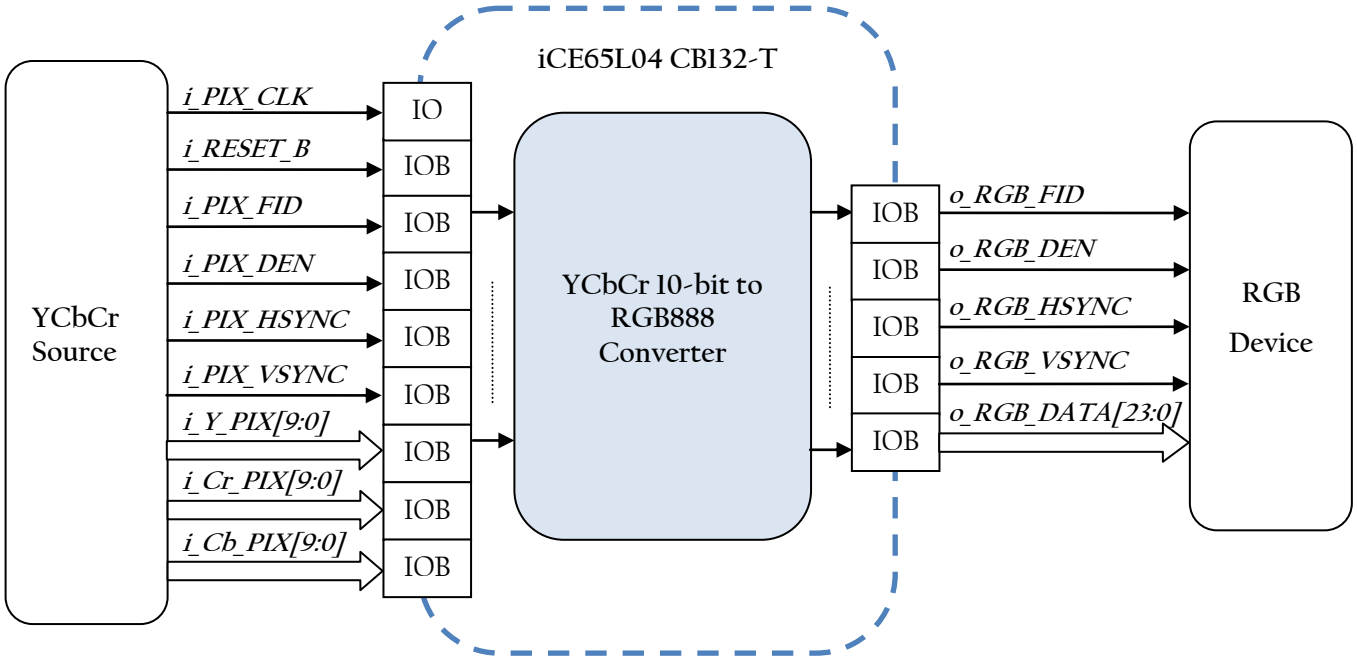
Resource Utilization

Table 1: **Resource Utilization**

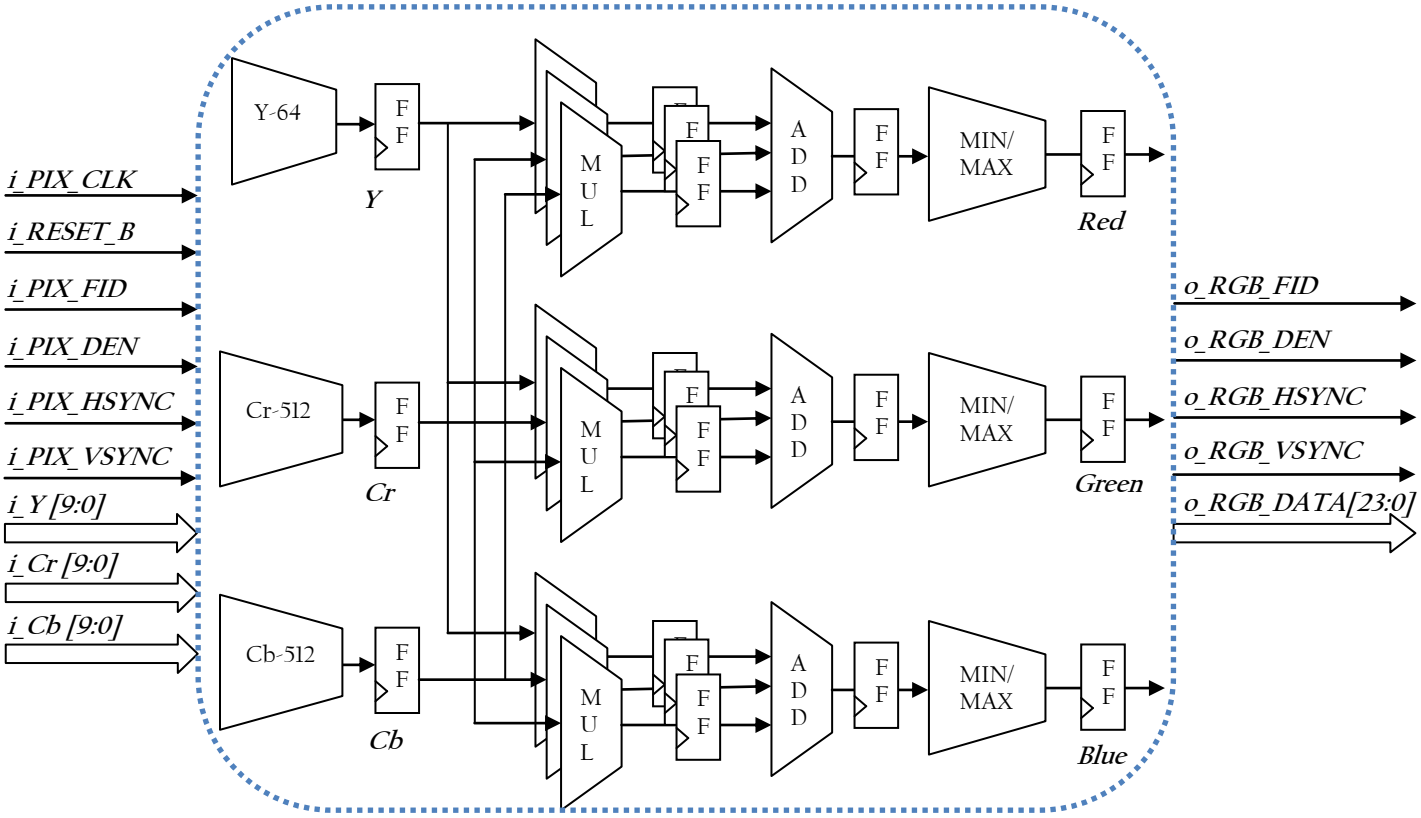
LUTs	Registers	Memory	I/Os	GBs
337	199	0	0	0

Note: Resource Utilization is based on iCEcube 2010.12.14671 release.

System Block Diagram



Functional Block Diagram



Design Interface

Signal Name	Pin Type	Signal Description
i_PIX_CLK	Input	Input Pixel Clock
i_RESET_B	Input	Active High asynchronous system reset
i_PIX_DEN	Input	Synchronous Data Enable(YCbCr valid)
i_PIX_HSYNC	Input	Horizontal Sync
i_PIX_VSYNC	Input	Vertical Sync
i_PIX_FID	Input	Input Frame ID(odd/even field indicator)
i_Y[9:0]	Input	Y component of Pixel
i_Cr[9:0]	Input	Cr component of Pixel
i_Cb[9:0]	Input	Cb component of Pixel
o_RGB_DEN	Output	RGB Data valid
o_RGB_HSYNC	Output	Pipelined Horizontal Sync
o_RGB_VSYNC	Output	Pipelined Vertical Sync
o_RGB_FID	Output	Output Odd/Even field indicator(pipelined)
o_RGB_DATA[23:0]	Output	Converted RGB pixel

Configurable Parameters

None

Register Map

This design does not have any user accessible registers or memory.

Design Details

This module converts 10-bit YCbCr 4:2:0 to RGB888 as per the following conversion expressions:

R = 1.164(Y-64) + 1.596(Cr-512)

G = 1.164(Y-64) - 0.813(Cr-512) - 0.392(Cb-512)

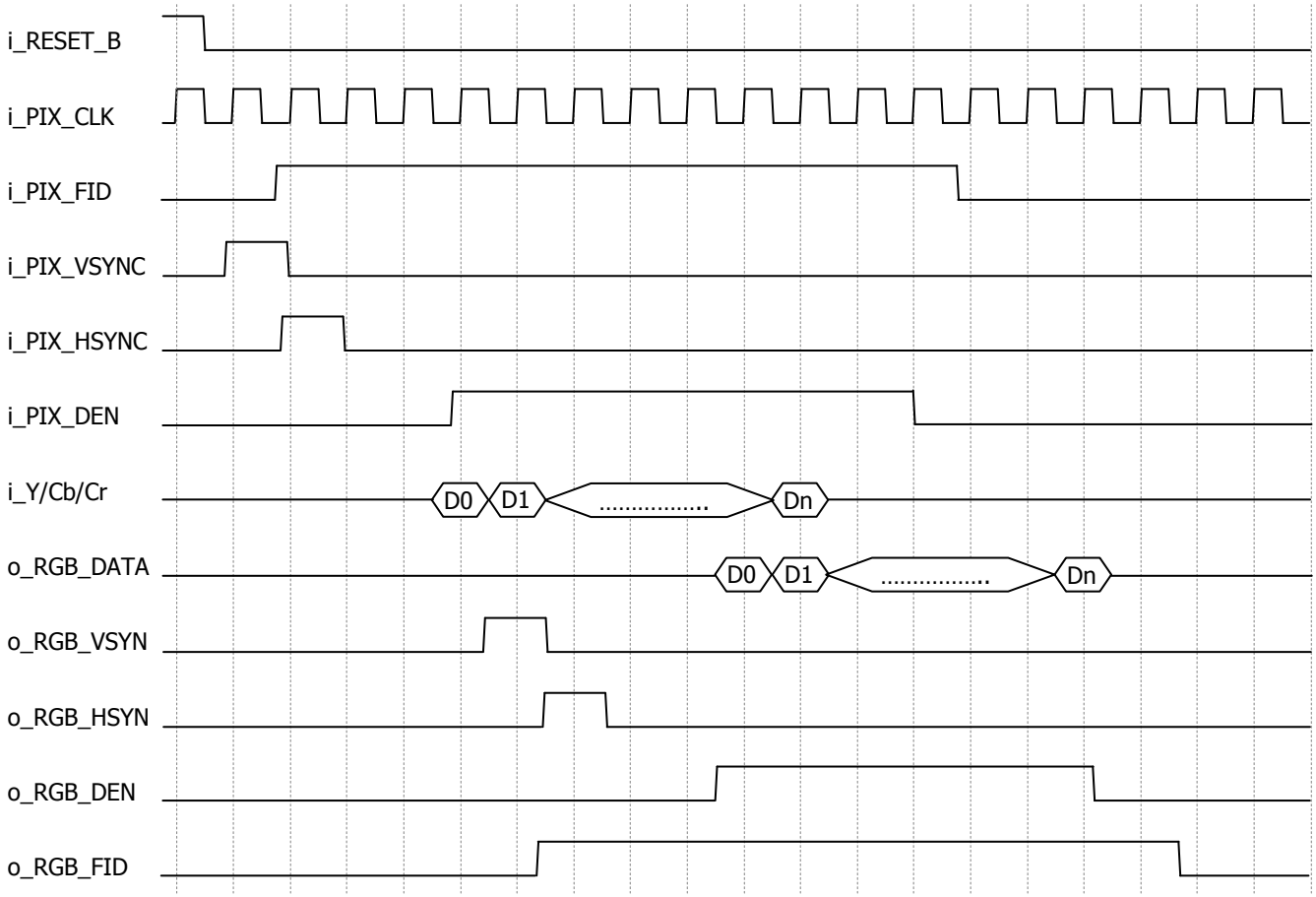
B = 1.164(Y-64) + 2.017(Cb-512)

The implementation comprises of a set of constant coefficient multipliers and add/sub logic arranged in pipelined fashion. Considering the large amount of data path involved here, a pipelined implementation is provided here to improve the performance. If the converted R, G and B values falls outside the allowed range, then the values are clipped and limited to the maximum/minimum possible range. This is a fully synchronous design and all the modules listed in the block diagram generates registered output through input pixel clock. To facilitate easy insertion to practical video systems, the design makes use of video synchronization signals pixel clock (i_PIX_CLK), valid data indicator (i_PIX_DEN) and generates a delayed version of i_PIX_HSYNC, i_PIX_VSYNC, i_PIX_DEN and i_PIX_FID so that control signals synchronized with the output RGB888 stream.

Initialization Conditions

This design does not have any user specific initialization conditions.

Timing Diagrams



Note: Signal naming here in the waveform is same as that listed in Pin Description table

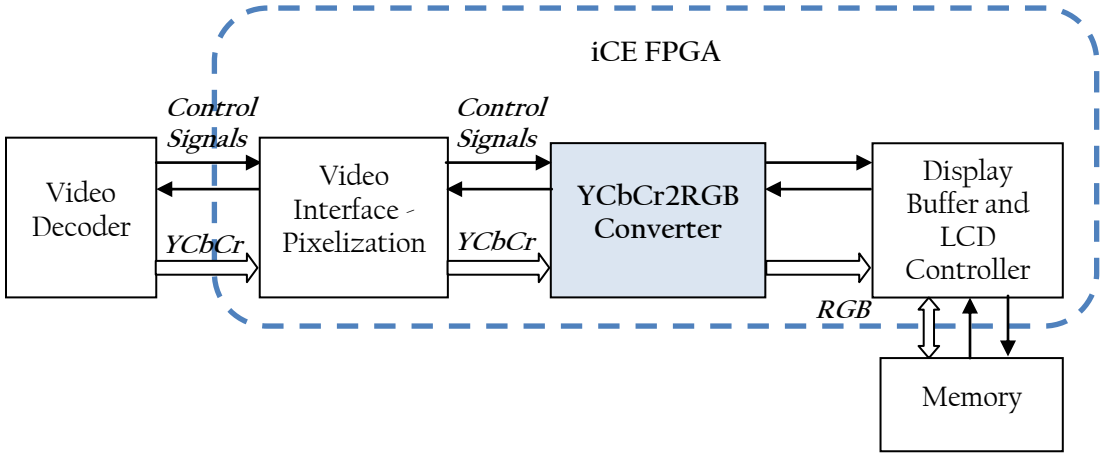
Bus Performance

The design can operate at maximum of 60MHz

Usage Examples

Common YCbCr video sources include NTSC video decoders, MPEG decoders, and cameras. YCbCr to RGB converters are useful in applications like Video Surveillance, Display Systems, Image/Video processing applications, Image decompression systems etc...

Example usage of this module is illustrated in the block diagram below, which interfaces NTSL/PAL/SECAM Video Decoder to a Display system. Video Pixelization module decodes YCbCr stream and generates HSync, VSync, DEN and FID control signals.



Simulation setup comprises of a testbench which provides input Y, Cb, Cr values for various colors like red, blue, green, white, black, cyan, magenta and yellow. The DUT generated output RGB888 values are compared against the corresponding known RGB888 values.

System Designer Flow

YCbCr10BitToRGB888 is compatible with System Designer/IP-XACT 1.2

The System Designer flow is as follows,

1. Launch the System Designer from Synplify Pro using menu 'Import -> Launch System Designer'.
2. Create a new project(open an existing old project, as necessary) and import the IP-XACT XML file
3. Drag and place the component from the 'Library' pane to the 'Design' pane
4. Click on the “Generate Files” button, which generates the necessary files required for synthesis and simulation.
5. Go to Synplify Pro and click on the “Run” button to synthesize the System Designer generated files. Synplify Pro generates all the necessary files for P&R in iCECube.

References

The following references were used in the creation of this design:

- SiliconBlue Technologies, Inc. "iCE65 Ultra Low-Power mobile FPGA Family" datasheet (26-May-2010).
- Wikipedia : http://en.wikipedia.org/wiki/YCbCr

Revision History

Version	Date	Description
1.0	25-OCT-2010	Initial draft document
1.1	07-DEC-2010	IP-XACT format Update

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