

Overview

Pulse Width Modulation (PWM) of a signal involves the modulation of its duty cycle, to convey either information over a communication channel or control the amount of power sent to a load. PWM is employed in a variety of applications, ranging from measurements and communications to power control and conversion, mainly because of its low power, noise-free and low cost characteristics.

In order to supply multiple PWM signals driving a number of power control applications, a cost-effective approach is required where one can have individual control over the duty cycle of each of the output PWM signals. This is a generic MxN PWM Controller, where the number of PWM outputs are configurable using generic parameters. This document provides a brief description of the Generic MxN Channel PWM Controller.

Features

- User configurable PWM Resolution
- Configurable PWM output channels
- IP-XACT version 1.2 compliant

Resource Utilization (for M = 3, N = 16)

Table 1: Resource Utilization

LUTs	Registers	Memory	GBs	I/Os
99	74	3	0	0

Note: Resource Utilization is based on iCECube 2010.12.14671 release.

System Block Diagram

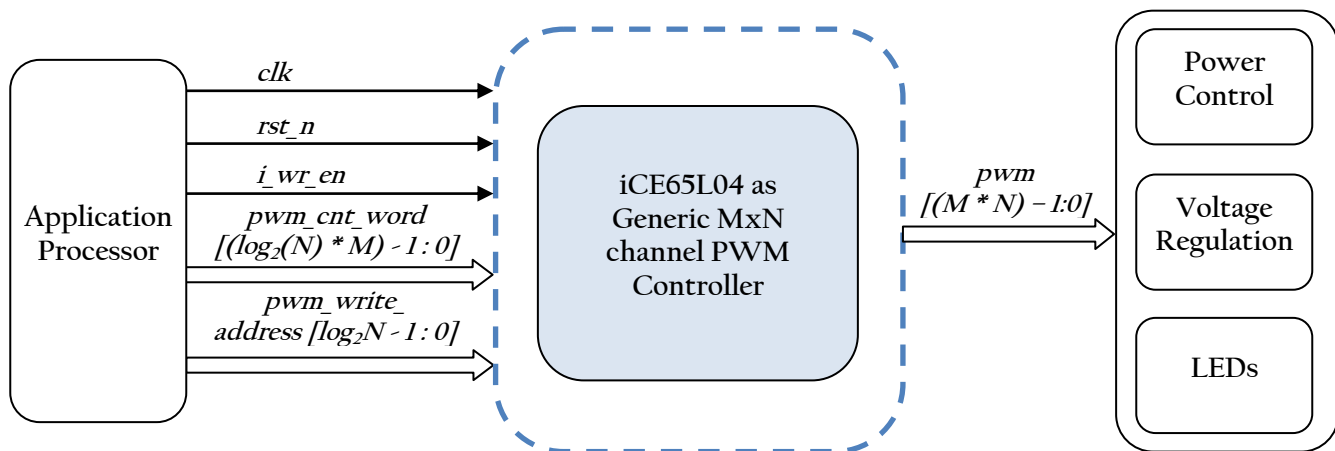


Figure 1: System Block Diagram

Functional Block Diagram

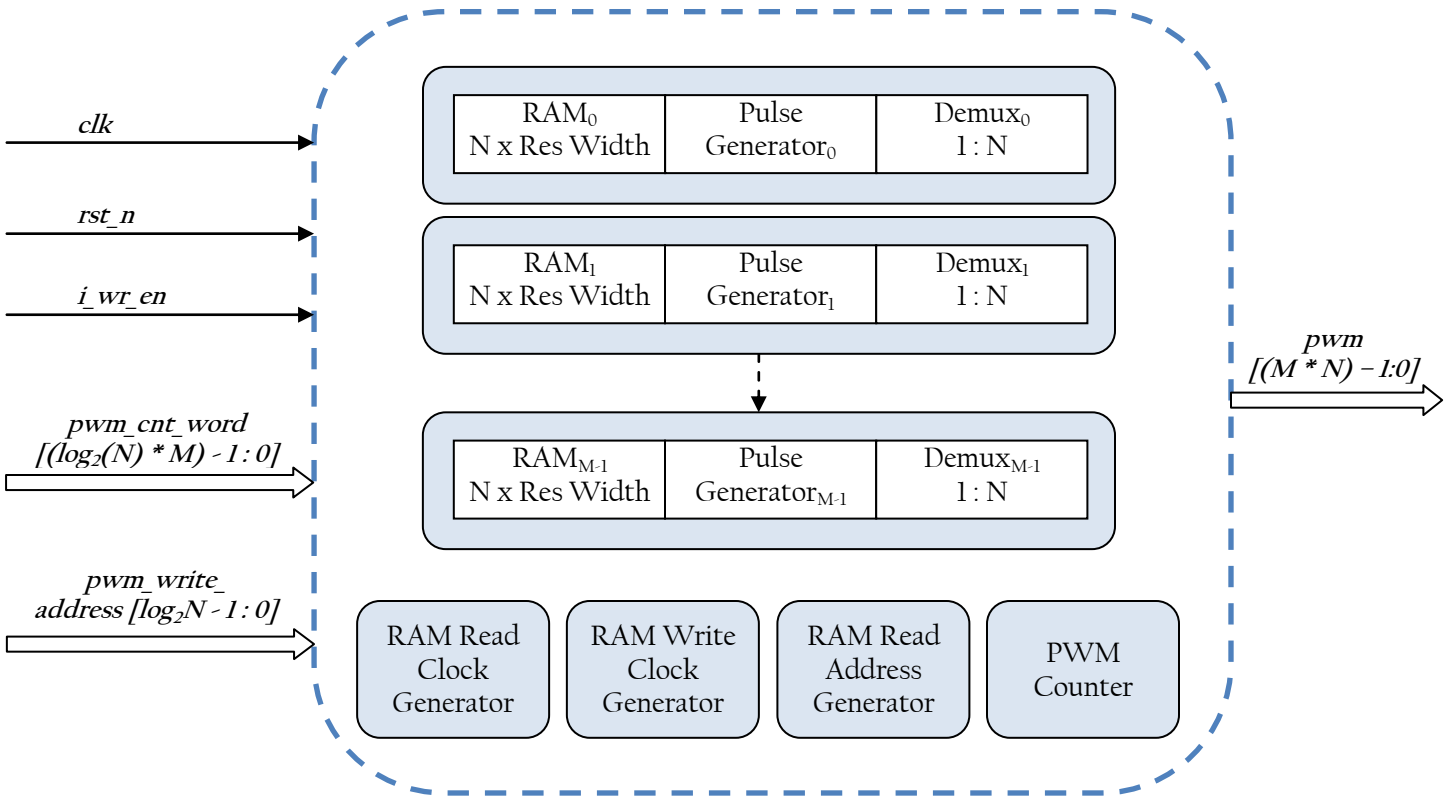


Figure 2: Functional Block Diagram

Design Interface

Table 2: Pin Description

Signal Name	Pin Type	Signal Description
clk	Input	System clock
rst_n	Input	Asynchronous Active Low System Reset
i_wr_en	Input	Active High Write Enable
pwm_cnt_word [11 : 0]	Input	Control Word
pwm_write_address [3 : 0]	Input	Write Address for the Control Word
pwm [47 : 0]	Output	PWM Signals

Configurable Parameters

None

Design Details

RAM : 'M' RAMs, each of size 'N' x PWM Resolution is used to store all the control words. The size of the RAM is dependent on the value of 'N' (number of output channels) and the PWM resolution required. All the 'N' control words are read in a single write clock cycle. Hence the write clock to the RAM is divided by a factor of 'N'.

Pulse Generator : This is required to compare the two input words (Control word from the RAM and the 'count' value from the Counter), and generate the PWM signal. If the Control word is greater than or equal to the 'count' value, the output is '0', otherwise it is '1'.

1 : N Demultiplexer : This is used to route the appropriate PWM signal to one of the 'N' output channels, using the read address of the RAM as the select line to the Demultiplexer.

Counter : This is a free running counter. The generated count value is compared with the control word from the RAM in order to generate the PWM signal. It is also used to generate the Read Address to the RAM. In Figure 2, it is depicted as PWM Counter and Read Address Generator

RAM Write Clock Generator : This divides the System Clock by a factor of 'N', so that for every write cycle (one Control word written to the RAM), there are 'N' read cycles ('N' Control words are read out from the RAM).

The values of 'N' are such that they have to be in powers of two i.e. 8, 16, 32 etc. This is because the size of the RAM depends on 'N'. 'M' can take any positive number. Examples can include 2 x 4, 5 x 32, 4 x 16 etc.

Usage Examples

Initialization Condition

When 'rst_n' is Low, 'pwm [47 : 0]' will be Low.

Example #1

Consider a 2 x 2 voltage regulator regulating voltage between 0V and 5V. In this case, we can assume M = 2 and N = 2. Hence, the Control word will be 2 bits long.

Table 3: Voltages generated for different Control words

Control Word	Duty Cycle (%)	Voltage Generated (V)
00	25	1.25
01	50	2.5
10	75	3.75
11	100	5

System Designer Flow

PWM MxN IP is compatible with System Designer/IP-XACT 1.2. The System Designer flow is as follows,

1. Launch the System Designer from Synplify Pro using menu 'Import -> Launch System Designer'.
2. Create a new project (open an existing old project, as necessary) and import the IP-XACT XML file
3. Drag and place the component from the 'Library' pane to the 'Design' pane
4. Click on the “Generate Files” button, which generates the necessary files required for synthesis and simulation.
5. Go to Synplify Pro and click on the “Run” button to synthesize the System Designer generated files. Synplify Pro generates all the necessary files for P&R in iCECube2.

References

The following references were used in the creation of this design:

- SiliconBlue Technologies, Inc. “[iCE65 Ultra Low-Power mobileFPGA Family](#)” datasheet (26-MAY-2010)

Revision History

Version	Date	Description
1.0	10-SEP-2010	Initial Draft Document
1.1	03-DEC-2010	IP-XACT format update

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